Design of a 600 W half bridge LLC converter using 600 V CoolMOS™ P7

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About this document

Scope and purpose

This application note will describe the design and performance of a 600 W LLC demo board. This is a high performance example with a complete Infineon solution, including high voltage (HV) and low voltage (LV) power MOSFETs, controllers, and drivers. This document demonstrates a very effective way to design the HV DC-DC isolation stage of a server PSU fulfilling the 80Plus® Titanium standard.

Besides design information and documentation for the LLC converter, the reader will receive additional information regarding how the 600 V CoolMOS™ P7 behaves in this LLC demo board and the benefits that will be achieved. The application note also provides suggestions on how to develop LLC converters in similar power ranges adapted to specific requirements.

Intended audience

This document is intended for design engineers who wish to evaluate high performance alternative topologies for medium to high power SMPS converters, and develop an understanding of the design process. Also, how to apply the somewhat complex LLC design methods to their specific system applications.

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1 Introduction

The reduction of size in power converters by increasing switching frequency and reducing magnetics component size is a goal that has been pursued for decades. The development of resonant converters with ZVS has been a cornerstone of this effort, but for a long time they have been considered as a way to “make good power solutions from mediocre semiconductors”, in fact limiting their usage. Moreover, with the advent of CoolMOS™ high performance silicon switches based on the superjunction concept, the improvements in Figure of Merit (FOM) reduced the need to use resonant topologies for many years. Now, the industry requirements for high efficiencies in converter performance, which drove a trend towards resonant switching square wave converters, such as the phase-shift full bridge converter, are creating a need for a closer look at the somewhat more difficult to design multiresonant LLC converter.

Classically, fully resonant converters have had a nominal disadvantage in conduction losses compared with soft switching square wave converters such as the phase shift full bridge, due to the difference in peak versus RMS current for sinusoidal current waveshapes versus trapezoidal. However, with the advent of the multi-resonant converter, it is possible with modern MOSFETs and their excellent FOM to achieve better optimized results with the LLC converter. This is in large due to the fact that the square wave converter is optimized at maximum duty cycle, which is only achieved at low line condition. Hence, to provide operational capability with typical Power Factor Correction (PFC) front ends, and some converter hold up time capability, they will typically need to be optimized for DC input as low as 325 V or 300 V, while they will normally operate at 380 V with a less favorable crest factor and higher net RMS current.

In contrast, an LLC converter can be optimized for the nominal DC input voltage, and use the boost up mode below the main resonance to achieve low line regulation with proper design. Combine this with a favorable silicon Bill of Material (BOM) situation, compared with a phase shift full bridge topology, the proper design approach, and a high performance converter is readily within reach.

In Figure 1, there is a synthetic comparison of several FOM metrics based on cost and performance between the phase-shift full-bridge converter and the LLC half bridge .

It can be seen in the first topology (blue arrows) retains some important features especially in controllability and flexibility with wide output regulation range, but the HB LLC (red arrows) provides some very important benefits in a modern SMPS design, including reduced BOM, easier ZVS and better performance synchronous rectification.

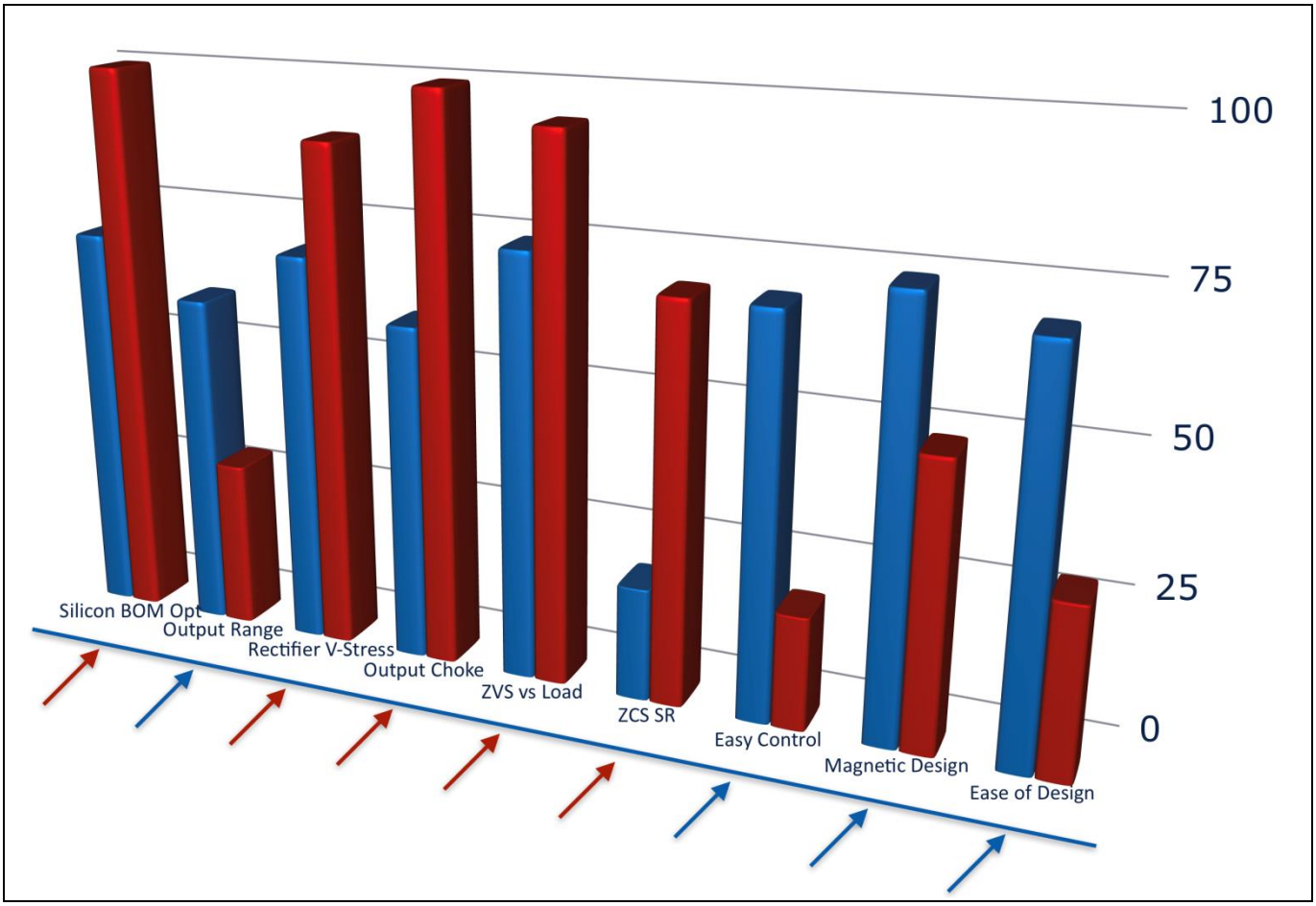


Figure 1 Comparison of several FOM metrics based on cost and performance between the phase-shift full-bridge converter and the LLC HB.

The principles of operation for the LLC converter will be examined in the next section, and the main tank design concepts reviewed. This will be followed by detailed design methodologies using both First Harmonic Approximation (FHA) and supplemented by exact design concepts.

The scope of this document is to describe the details of an analog controlled 600 W HB LLC demo board fully designed using Infineon products. (Order information in ISAR: EVAL_600W_12V_LLC_P7)

The target efficiency of this design is determined according to the need to fulfill (for the complete PSU) the 80+ Titanium standard; meaning certain minimum efficiency requirements for the HV DC/DC stage are fixed at 10%, 20%, 50% and 100% load conditions.

2 HB LLC converter principles of operation

The typical modes of operation of the LLC converter will be discussed in this chapter using an initial description of the concept behind FHA. The reasoning behind the basic configuration of the resonant tank will be introduced shortly. Finally, the concepts and challenges for successful implementation of synchronous rectification will be outlined.

The most important concepts are referred to here, in order to better understand the design considerations.

2.1 Tank configuration and operational modes

The principle schematic of a HB LLC converter is shown in Figure 2.

C_r, L_r and L_m represent the “resonant tank”. Together with the main transformer, they are the key components in the LLC design.

The primary HB and the output rectification are the other two stages to be defined.

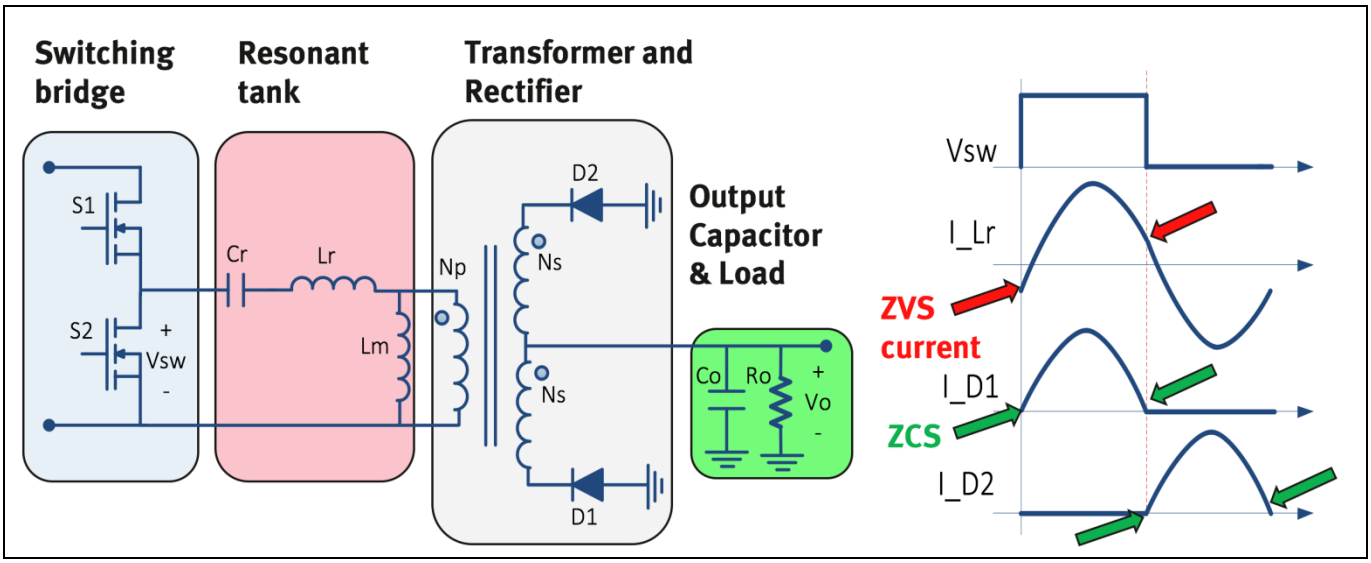


Figure 2 Principle schematic of a HB LLC converter

The LLC is a resonant converter that operates with frequency modulation instead of the PWM traditional approach to power conversion.

Figures 3, 4, 5 and 6 explain the fundamental operating mode of a HB LLC converter in a graphic format.

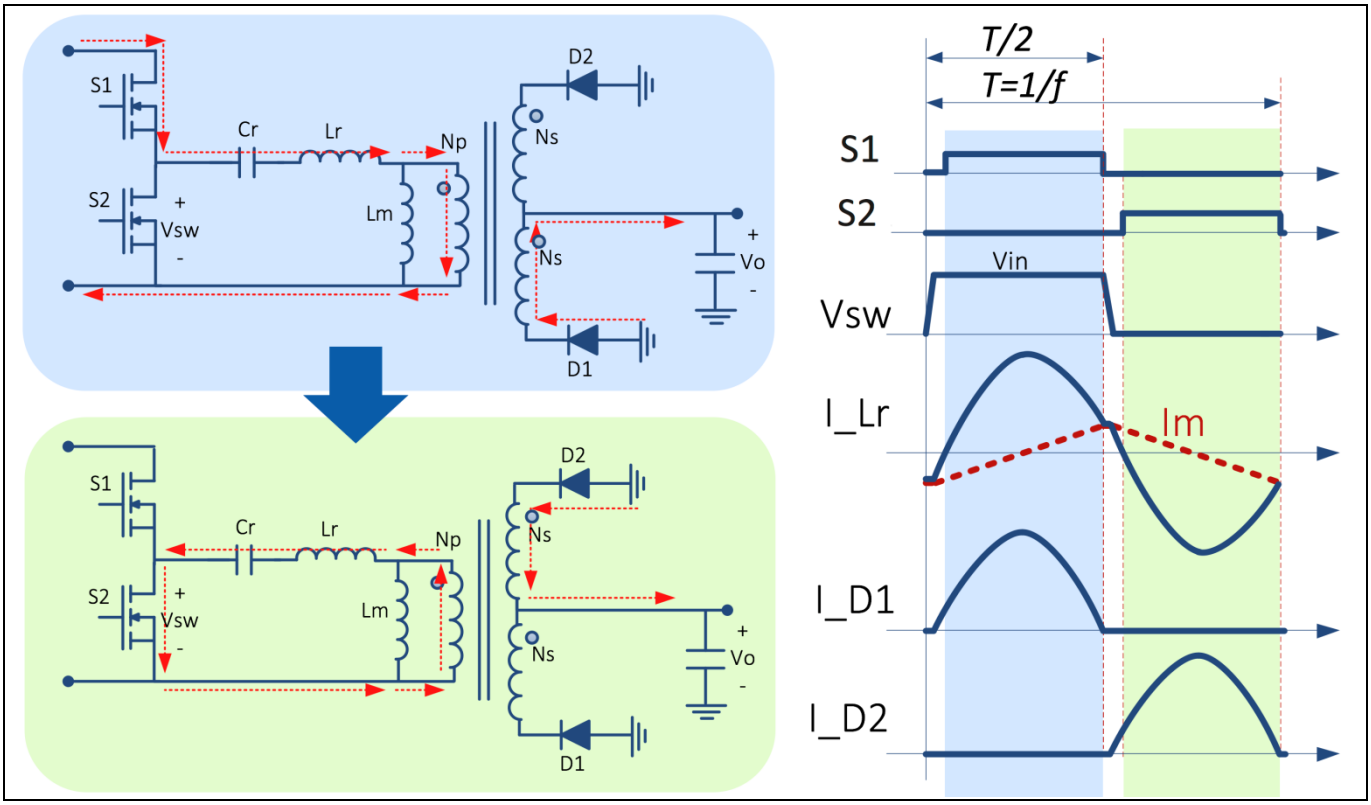


Figure 3 **Fully resonant operating mode, at the resonant point for C_r and L_r, with near ZCS turn-off of the primary side MOSFETs.**

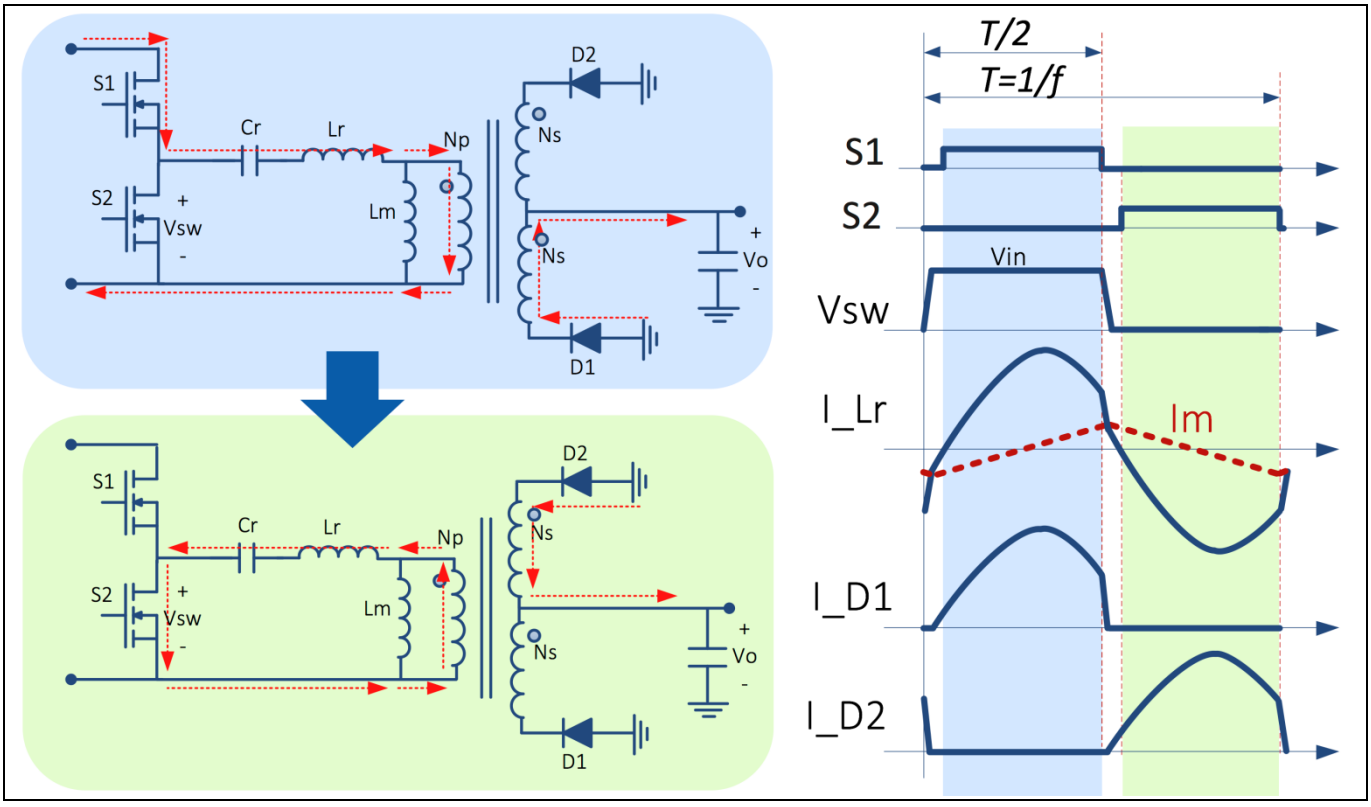


Figure 4 **Over resonant operation, above C_r-L_r resonance, for both half cycles, showing tank current waveforms and non-ZCS turn-off of the primary side MOSFETs**

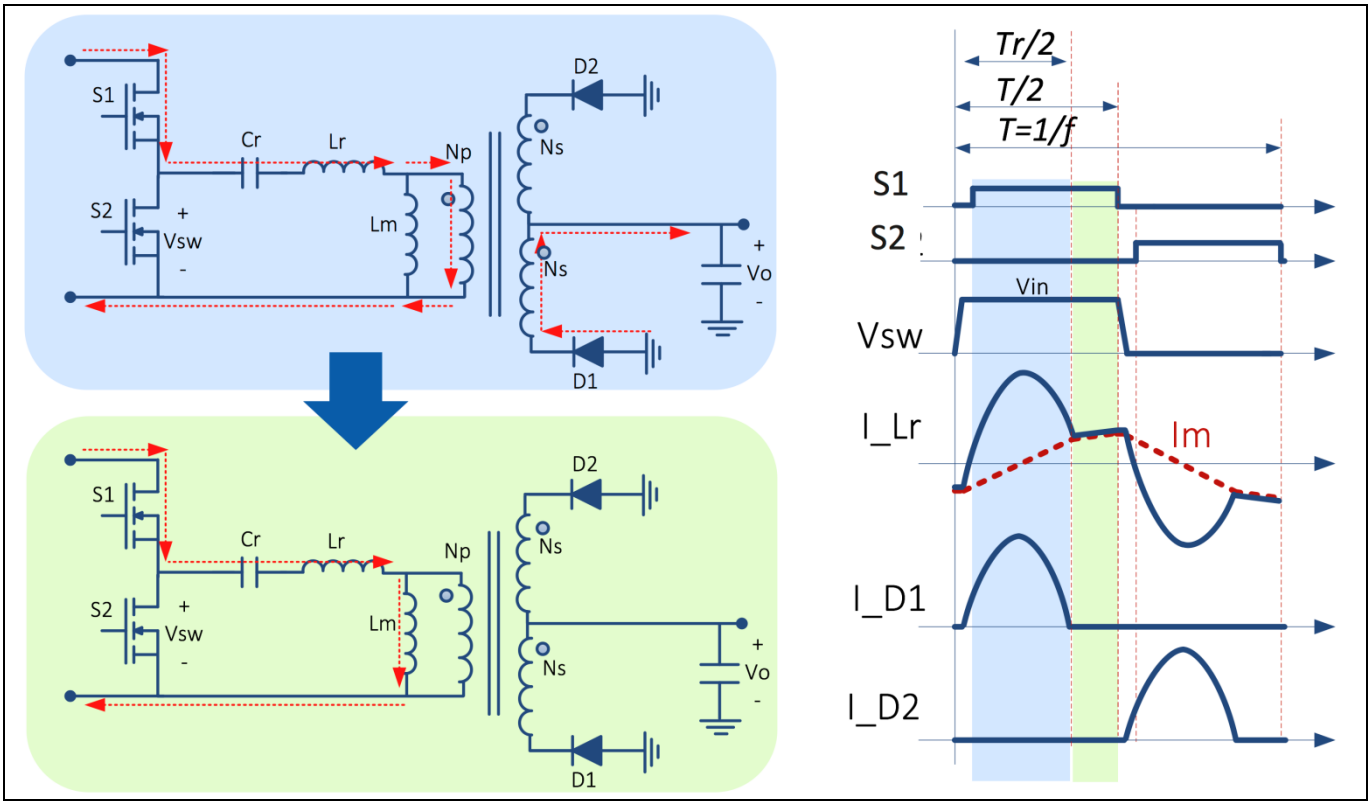


Figure 5 **Under resonant Discontinuous Current Mode (DCM) operation, (between the resonant point of C_r and L_r, versus the resonant point of C_r and L_r+L_m) half cycle 1**

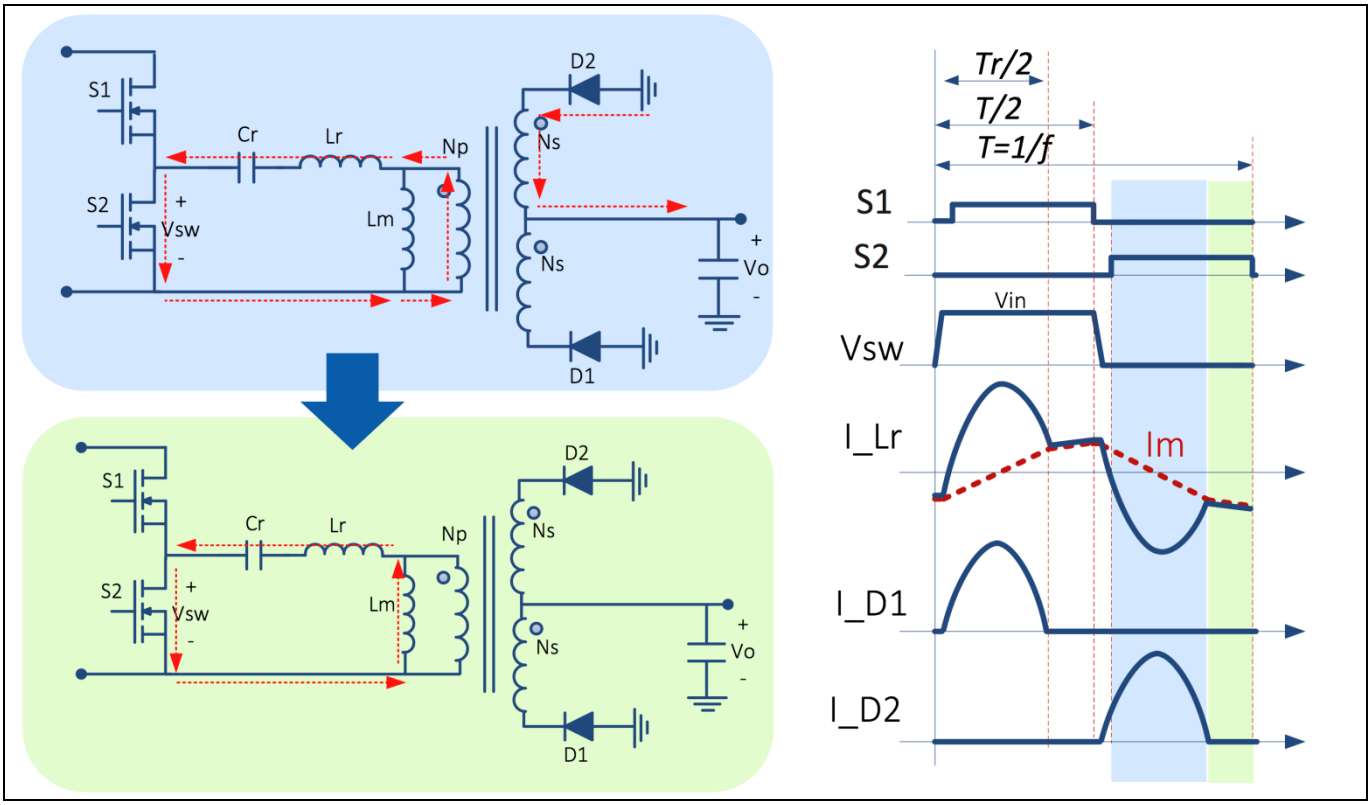


Figure 6 **Under resonant DCM mode operation, (between the resonant point of C_r and L_r, versus the resonant point of C_r and L_r+L_m) 2nd half cycle**

2.2 Analysis of the basic tank characteristics using FHA

The starting point in a resonant converter design is the definition of an energy transfer function, which can be seen as a voltage gain function, or a mathematical relationship between the input and output voltages of the converter. Trying to obtain this function in an exact way involves several nonlinear circuit behaviors governed by complex equations. However, under the assumption that the LLC operates in the vicinity of the series resonant frequency, important simplifications can be introduced.

In fact, under this assumption, the current circulating in the resonant tank can be considered purely sinusoidal, ignoring all higher order harmonics: this is the so-called First Harmonic Approximation method (FHA method), which is the most common approach to the design of an LLC converter.

In the FHA, the voltage gain is calculated with reference to the equivalent resonant circuit shown in Figure 7.

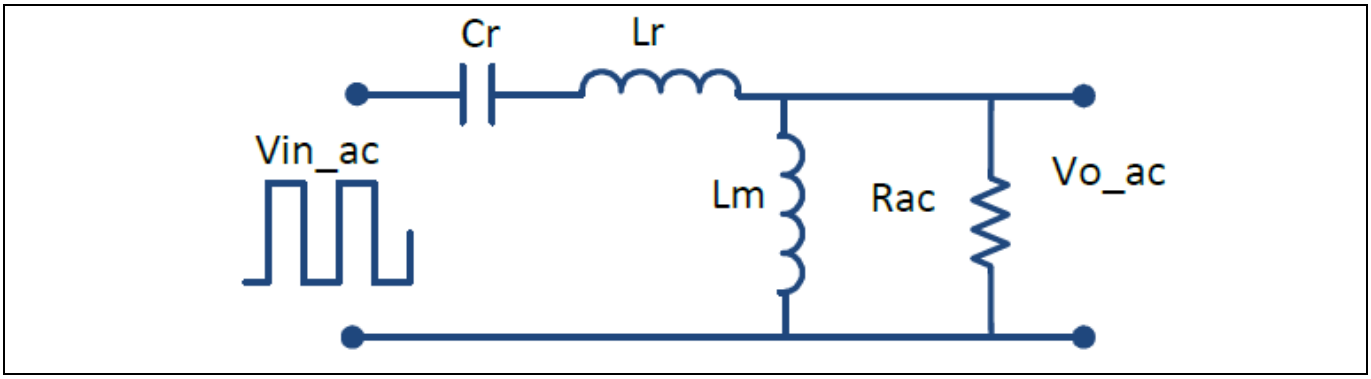


Figure 7 FHA equivalent resonant circuit

The mathematical expression for the gain (K) is given in terms of a normalized resonant frequency F_x:

$$K(Q,m,Fx) = \left|\frac{V_{o_ac}(s)}{V_{in_ac}(s)}\right| = \frac{F_x^2(m-1)}{\sqrt{(m\cdot F_x^2-1)^2 + F_x^2\cdot(F_x^2-1)^2\cdot(m-1)^2\cdot Q^2}} \quad (1)$$

Where:

$$m = \frac{L_r + L_m}{L_r}; \qquad f_r = \frac{1}{\sqrt{L_r\cdot C_r}}; \qquad Fx = \frac{f_s}{f_r}; \qquad R_{ac} = \frac{8}{\pi^2}\cdot\frac{N_p^2}{N_s^2}\cdot R_o; \qquad Q = \frac{\sqrt{L_r/C_r}}{R_{ac}}; \quad (2)$$

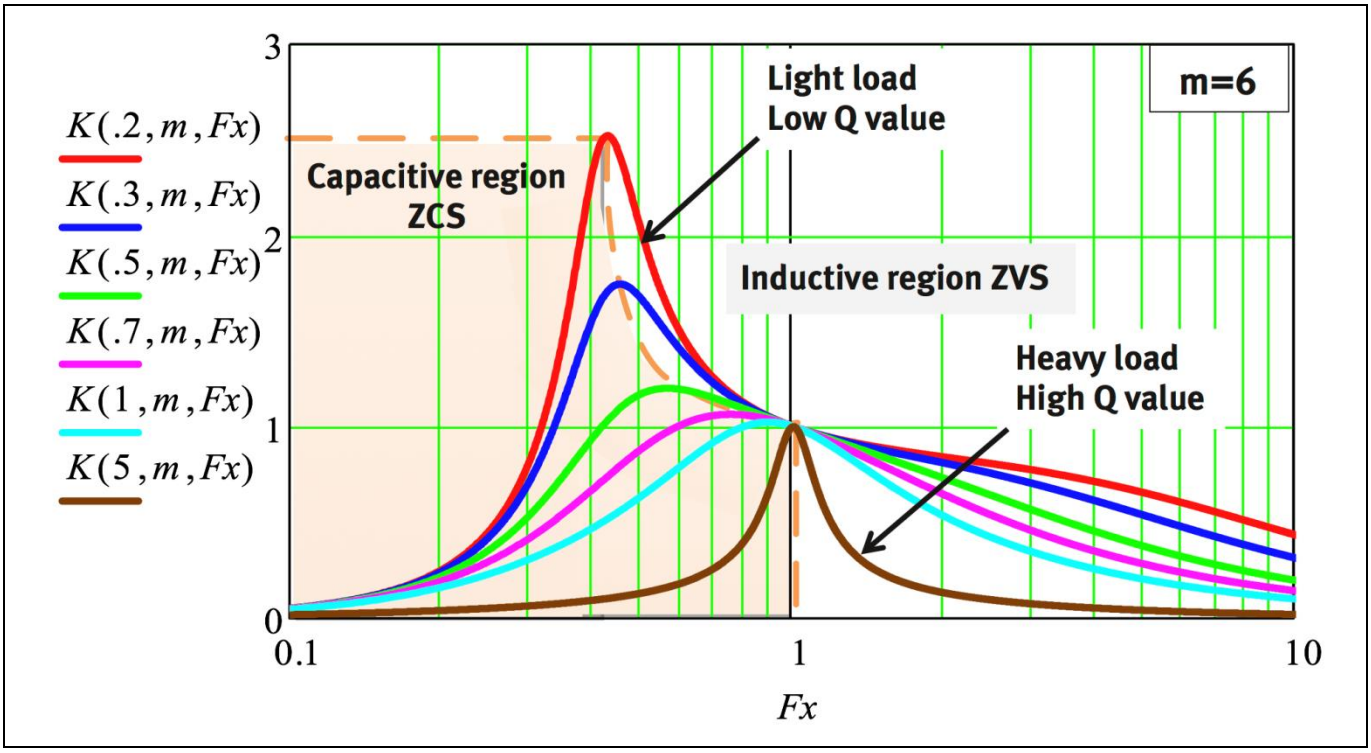


Figure 8 **Family of Q curves for a fixed m inductance ratio of 6**

2.3 Tank Q values and m inductance ratio: system implications

The resonant tank gain K can be plotted as a function of the normalized driving frequency F_x for different values of the quality factor Q and any single value of the inductance ratio factor m.

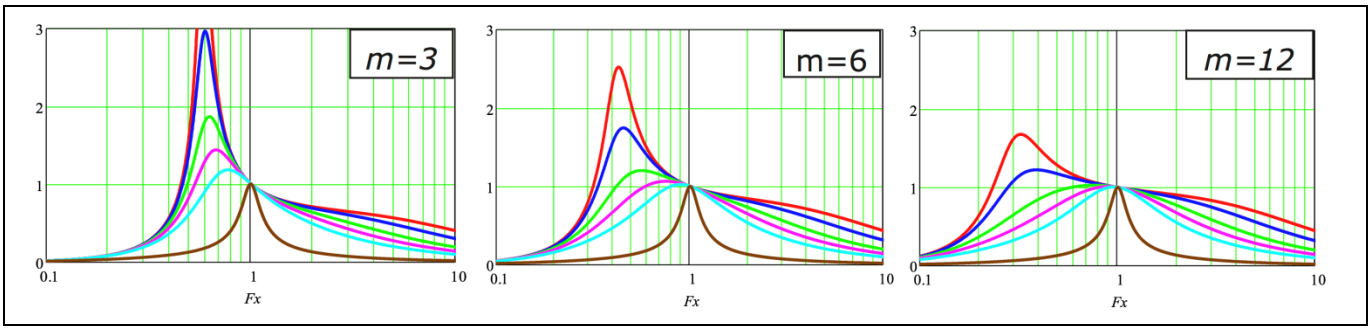


Figure 9 **Family of Q curves for m inductance ratios of 3, 6 and 12**

2.4 Benefits of split capacitor C_r

The design described in this document uses the configuration shown in Figure 10, typically known as the “split resonant capacitor technique”. This solution provides a couple of important benefits.

The first benefit is the reduction of the AC current stress on the resonant and input bulk capacitors, with consequent relaxed AC current requirements on those components, thereby achieving cost reduction and extended lifetime.

The second benefit involves the often critical LLC start-up sequence.

In fact, the split capacitor technique provides the possibility to charge the resonant capacitance simultaneously to the input bulk cap, thus reducing the required charging time. In fact, until the resonant capacitor is completely charged, the transformer is not driven symmetrically, so there is a significant difference in the up and down slopes of the resonant current and the current may not reverse in a switching half cycle. This condition could create a potentially damaging condition where a MOSFET is turned on while the body diode of the other HB MOSFET is conducting. This is the condition known as “hard commutation on the conducting body diode”, which submits the turning-off device to heavy stress. This may happen for several cycles at converter start-up.

Using the split resonant capacitor technique, the risk of having hard commutation is significantly reduced when the HV DC/DC converter is powered up in a relatively short time after the input bulk capacitor has been charged to the DC link voltage.

It should be made clear that this technique only may reduce the possible occurrence of hard commutation, but does not guarantee 100% prevention.

A safe and reliable operation at start-up is only possible through a proper control algorithm and HV MOSFET driving technique, along with a power device with a rugged body diode.

For further details about this topic, please refer to the paragraph 4.4 of this document and [4}.

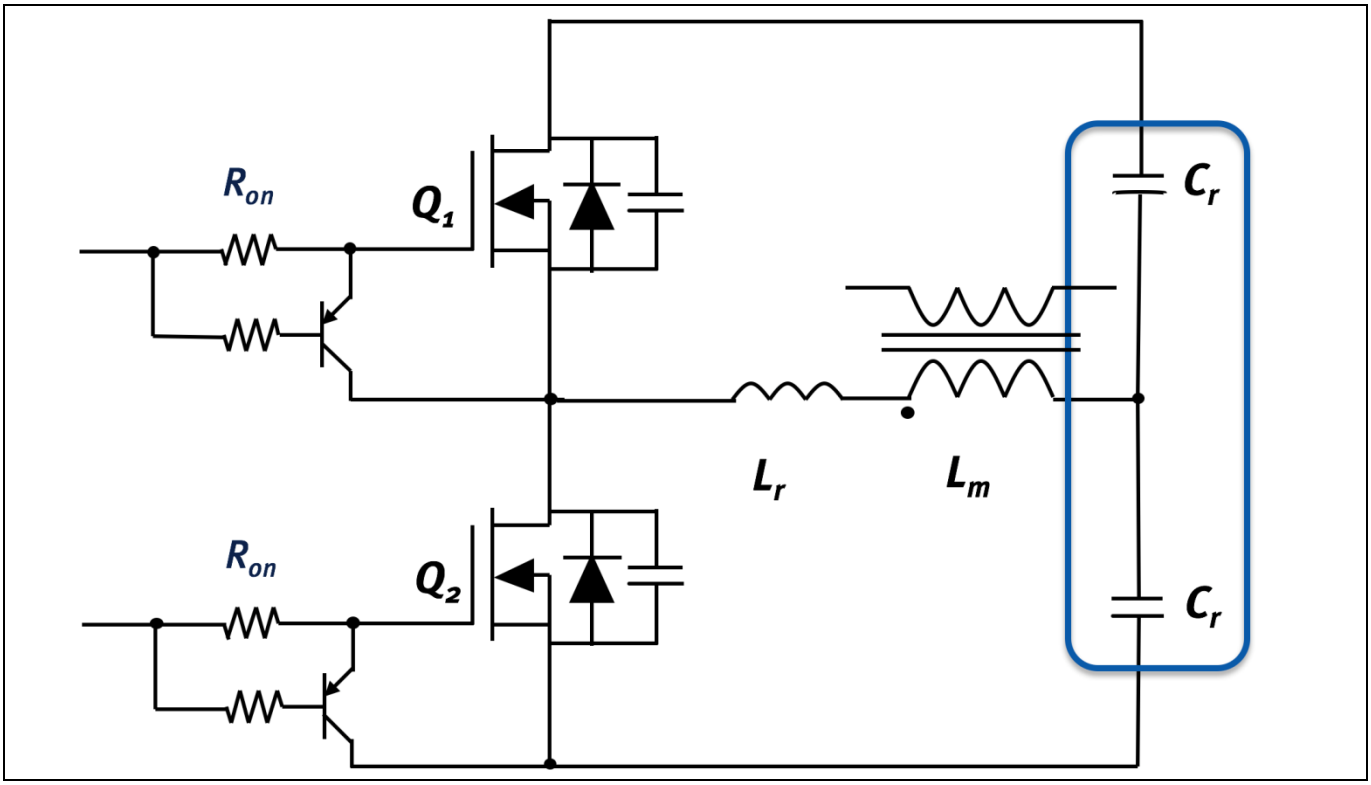


Figure 10 Re-arranging the resonant capacitor into a split capacitor HB configuration

2.5 Synchronous rectification concepts for LLC

Figure 11 briefly summarizes the technique to manage synchronous rectification in an HB LLC Converter

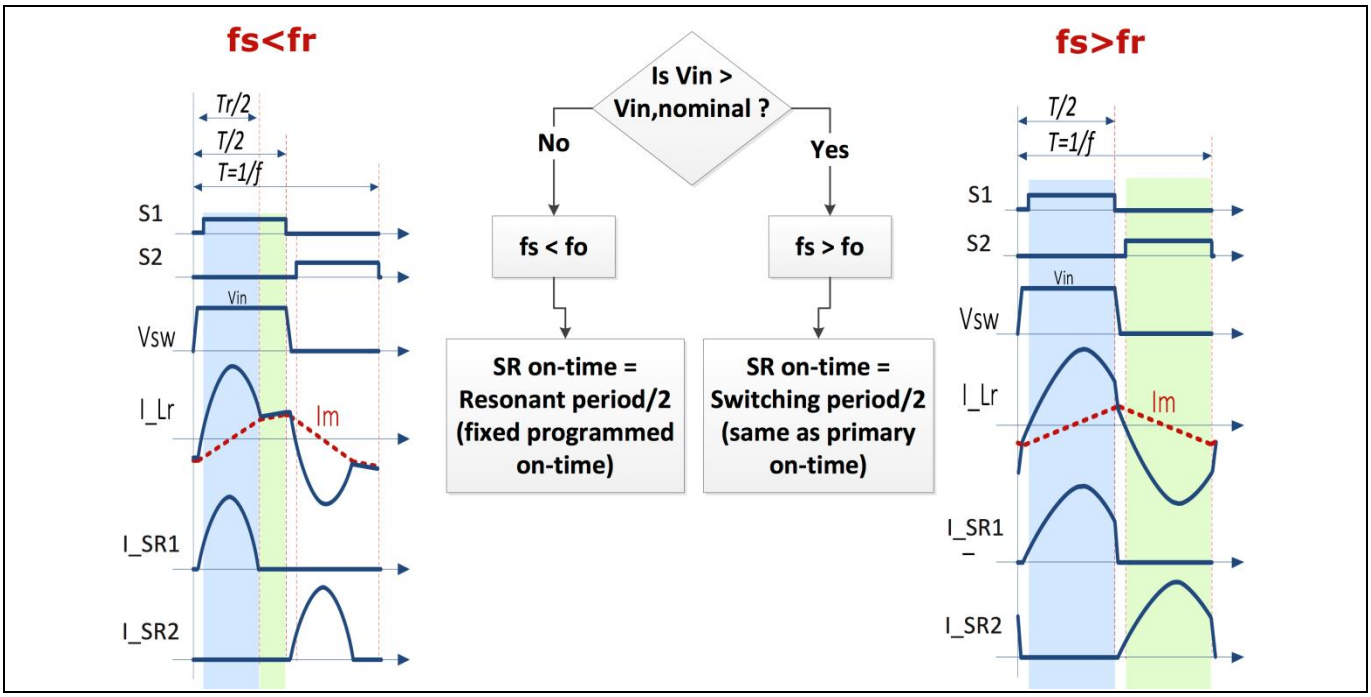


Figure 11 Synchronous rectification in an HB LLC Converter

3 LLC design methodologies for specific application requirements

An optimization procedure for the selection of the main LLC parameters, for both the FHA method and using exact calculation or simulation will be shown in the next section. The goal will be to achieve the best performance while fulfilling input and output regulation requirements.

At the same time, ZVS operation of the primary HB MOSFETs must be ensured in order to get full benefits from the soft switching behavior, especially at light load.

3.1 Input design data

In Table 1, an overview of the major design parameter is displayed.

Table 1 Design parameters

Description	Minimum	Nominal	Maximum
Input voltage	350 V_{DC}	380 V_{DC}	410 V_{DC}
Output voltage	11.9 V_{DC}	12 V_{DC}	12.1 V_{DC}
Output power			600 W
Efficiency at 50% P_{max}	97.4%		
Switching frequency	90 kHz	150 kHz	250 kHz
Dynamic output voltage regulation (0-90% Load step)			Max. overshoot =0.1 V Max. undershoot=0.3 V
V_{out_ripple}			150 mV_{pk-pk}

From the table above, the first important design parameters can be derived:

Main transformer turn ratio

$$n = \frac{N_p}{N_s} = \frac{V_{in_nom}}{2 \cdot V_{out_nom}} \approx 16 \quad (3)$$

Minimum needed gain

$$K_{\min}(Q, m, F_x) = \frac{n \cdot V_{o_\min}}{V_{in_\max}/2} \approx 0.95 \quad (4)$$

Maximum needed gain

$$K_{\max}(Q, m, F_x) = \frac{n \cdot V_{o_\max}}{V_{in_\min}/2} \approx 1.08 \quad (5)$$

3.2 Gain curve

The resulting gain curves, Figure 12, for loads between 10% and 100% of P_{max} are shown in the following plot:

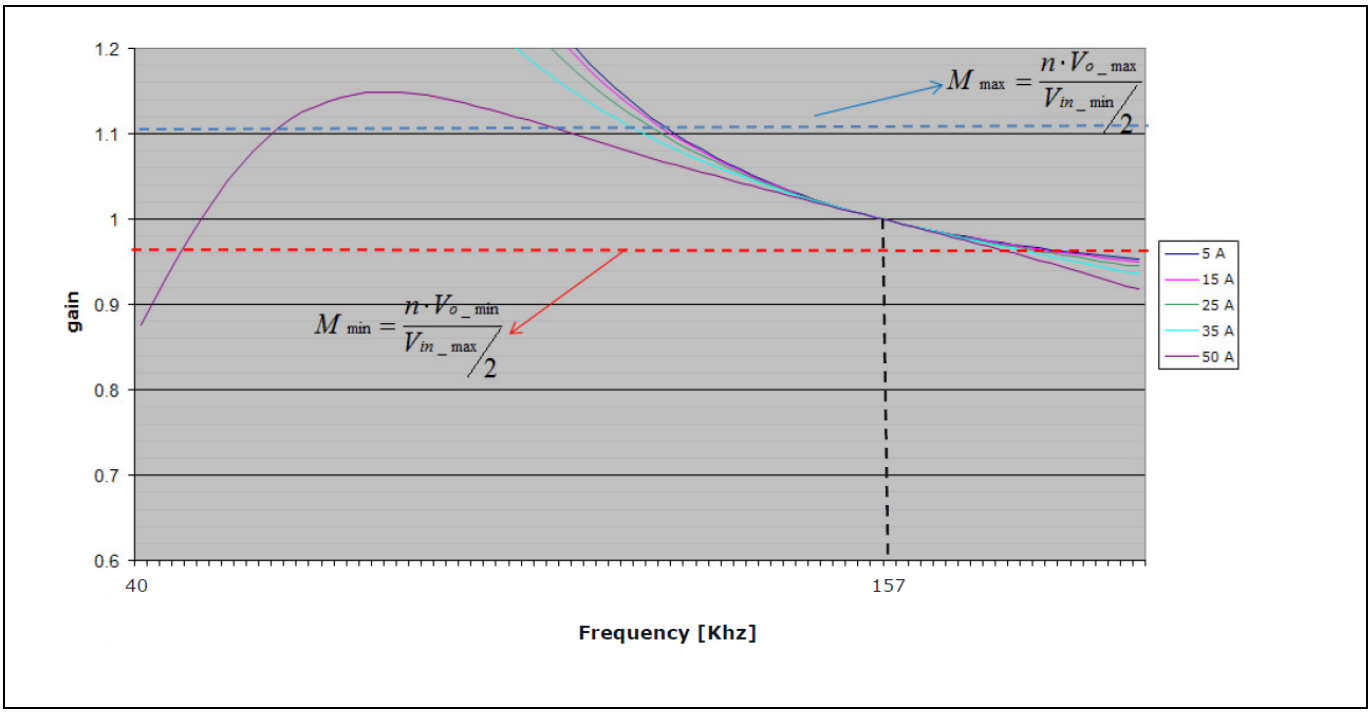


Figure 12 Gain Curve

Both the M_{min} and M_{max} limits cross all the gain curves of our LLC converter, meaning that the input / output regulation is fully achieved in the specified ranges.

3.3 Suggested FHA optimization process

Figure 13 shows a flowchart including all the steps in the design of a HB LLC converter.

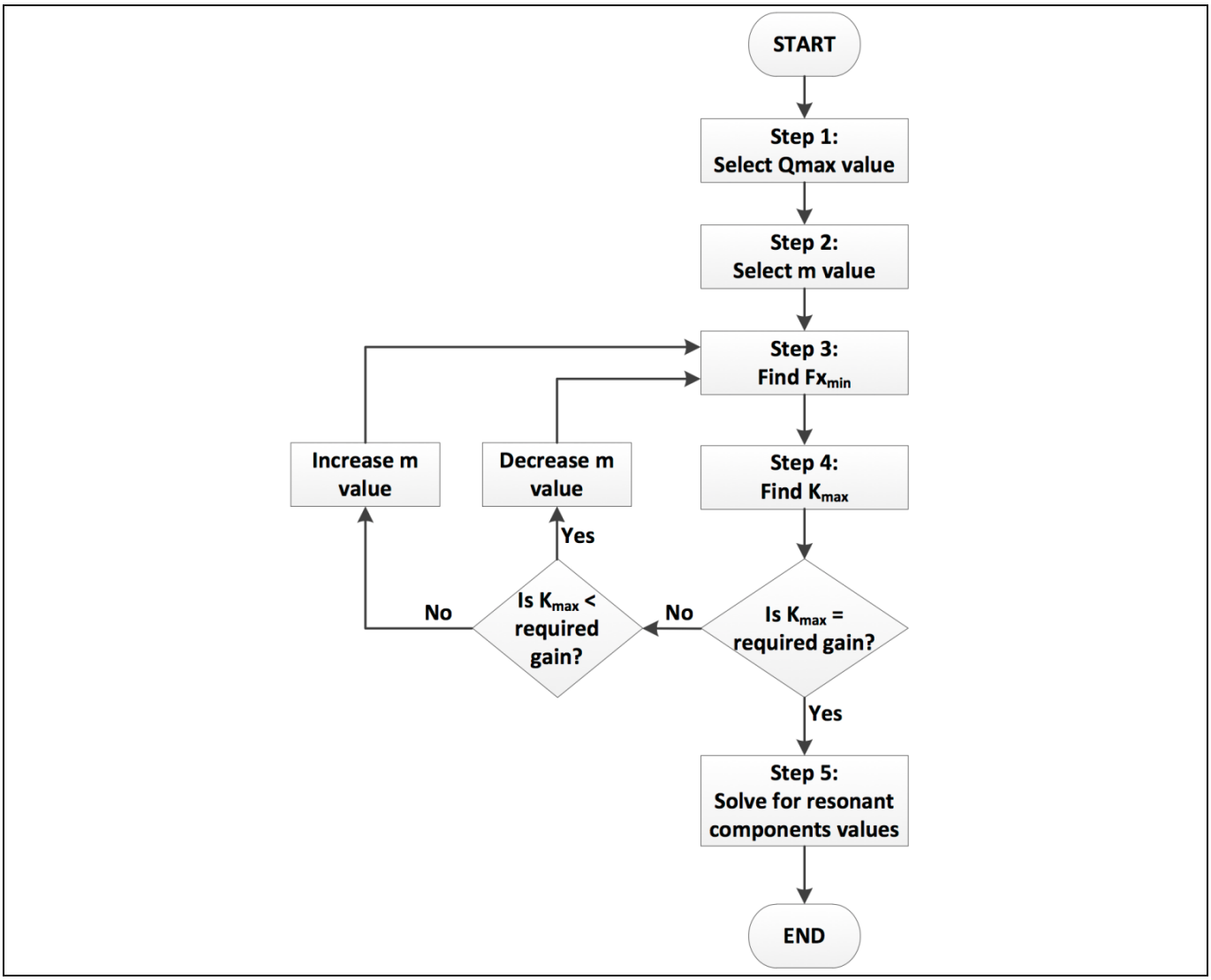


Figure 13 Suggested FHA optimization process

For all the details of this method, refer to [2]

3.4 Notes on the selection of the inductance factor (m)

The inductance factor (Equation 2) has an important impact on the converter operation. Lower values of m achieve higher boost gain and a narrower range of frequency modulation, meaning more flexible control and regulation, which is valuable in applications with very wide input voltage range.

On the other hand, this also means smaller values of $L_{m,}$ which leads to significantly high magnetizing current circulating in the primary side. This current does not contribute to the power transferred, but mainly generates conduction losses on the primary side.

In other words, there is a trade-off between flexible regulation and overall efficiency requirements, especially at light load.

In the case of the demo board described in this document, the main goal is to achieve high efficiency, so a relatively high m is selected. This minimizes the circulating current from the magnetizing inductance. This is permitted as the stated input range is relatively narrow, and a higher value of L_m will be acceptable as long as sufficient current is available to achieve resonant transitions under light load conditions.

We rely on the bulk capacitor in the case of specific hold up time requirements at the complete AC/DC SMPS level. However, high density designs may not permit this, as the bulk capacitor does not reduce in size with increasing switching frequency. In some cases, adjustment of the input voltage range may be needed.

In this case, the chosen value is **m≈12**.

3.5 Resonant components calculation

Combining equations (1) and (2), we get a system where the unknown variables are L_r, C_r and L_m

Solving it means the following values are set for the LLC converter:

$$n = \frac{Np}{Ns} = \frac{V_{in_nom}}{2 \cdot V_{out_nom}} \approx 16 \Rightarrow Np = 16; Ns = 1 \quad (6)$$

$$m = \frac{Lr + Lm}{Lr} \approx 12 \Rightarrow Lm = 195\mu H; Lr = 17\mu H \quad (7)$$

$$Cr = 66nF \quad (8)$$

$$fr = \frac{1}{2\pi \cdot \sqrt{Lr \cdot Cr}} \approx 150KHz \quad (9)$$

3.6 The ZVS behavior: energy and time considerations

The ZVS calculations involve two types of analysis, one in the energy domain and the other in the time domain. The goal is to have enough energy in the resonant tank to be able to discharge the output capacitance of the primary MOSFET, but also maintain an appropriate dead time between the two devices.

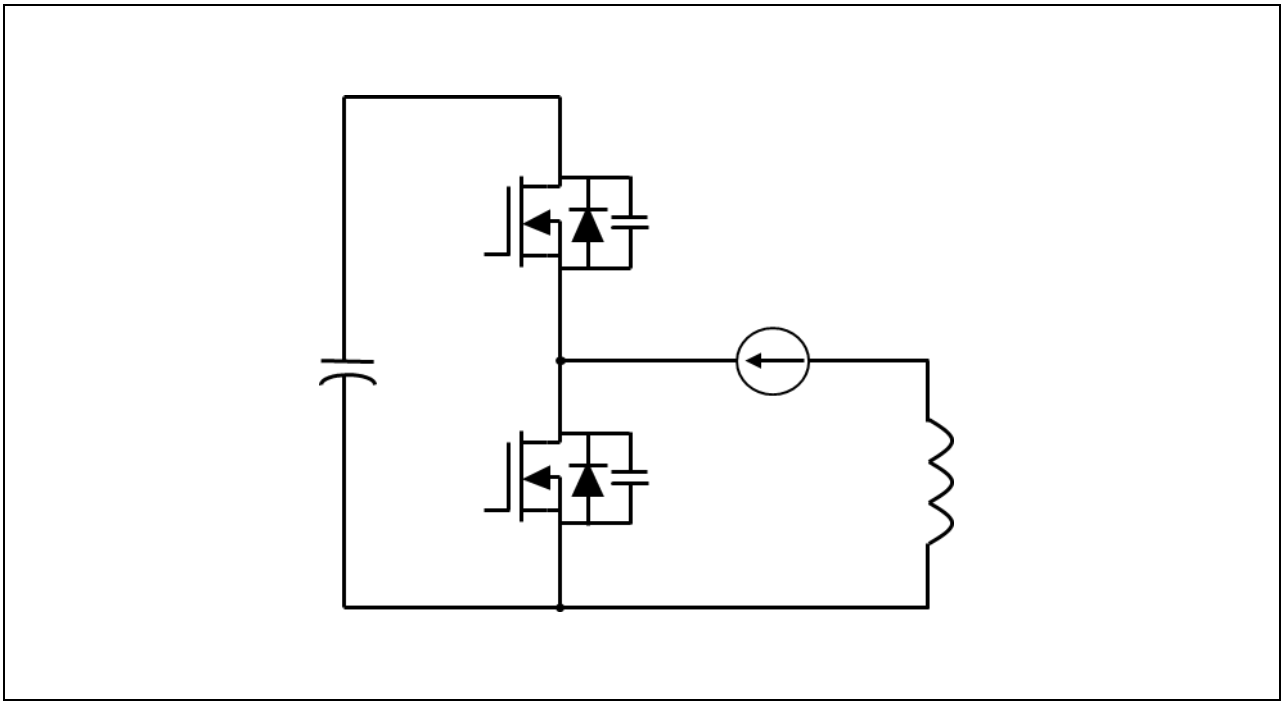


Figure 14 Equivalent circuit in resonant drain to source transitions

The two key parameters in our analysis are the following:

$C_{o(er)}$ is the C_{oss} energy related component of the HV MOSFET used, in this case IPP60R180P7.

Q_{oss} is the charge stored in C_{oss} at $V_{in(nom)}$ = 380 V_{DC}. Q_{oss} is linked to $C_{o(tr)}$ by the formula

$Q_{oss} = C_{o(tr)} * V_{in(nom)}$

$C_{o(er)}$ and $C_{o(tr)}$ are the effective output capacitances of the MOSFET, respectively energy and time related.

3.6.1 Energy related equations

$$I_{mag_min} = \frac{2\times\sqrt{2}}{p}\times\frac{n\times V_o}{2p\times f_{sw_max}\times L_m} = 0.672A \quad (10)$$

$$En_{res_min} = \frac{1}{2}\cdot(Lm+Lr)\cdot I^2_{mag_min} = 95.1\mu J \quad (11)$$

$$En_{cap_max} = \frac{1}{2}\cdot(2C_{o(er)})\cdot V^2_{DS_max} \approx 9\mu J \quad (12)$$

$$\Rightarrow En_{res_min} > En_{cap_max} \quad (13)$$

3.6.2 Time related equations

It can be demonstrated that:

$$t_{dead} = \frac{t_{ecs}}{2} + \frac{2 \cdot Q_{oss,\,@\,400V}}{\mathrm{I}_{m,\,pk}} \tag{14}$$

where t_{dead} is the dead time set between the conduction time of the two HB devices and t_{ecs} is the time when the channel of each MOSFET remains in conduction after turning it off (linear mode operation), which is a function of device parameters including $V_{gs(th)}$, $R_{g(tot)}$ and C_{gs}/C_{gd}.

Using the formula above, together with the min. and max. values of the magnetizing current and considering t_{ecs}=10 nsec:

$$\mathrm{I}_{mag_min} = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot V_o}{2\pi \cdot f_{sw_max} \cdot L_m} = 0.672A \tag{10}$$

$$\mathrm{I}_{mag_max} = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot V_o}{2\pi \cdot f_{sw_min} \cdot L_m} = 1.66A \tag{11}$$

$$t_{dead,\,min} = \frac{t_{ecs}}{2} + \frac{2 \cdot Q_{oss,\,@\,400V}}{\mathrm{I}_{m,\,ag,\,max}} \approx 130n\mathrm{sec} \tag{14}$$

$$t_{dead,\,max} = \frac{t_{ecs}}{2} + \frac{2 \cdot Q_{oss,\,@\,400V}}{\mathrm{I}_{mag,\,min}} \approx 311n\mathrm{sec} \tag{15}$$

3.7 The main transformer design

The most critical condition for the main transformer is full load, mainly for thermal reasons. The selection of the core size and material is based on this condition along with the power density target (thereby including switching frequency) and the available airflow.

Keeping sufficient margin in the design, the minimum efficiency requirement at full load is fixed for the HB LLC converter at 97%, which means the goal is to keep the total dissipated power in that condition below 18 W.

In order to guarantee a balanced spread of power and heating, a good rule in the design of the LLC converter is to keep the total power dissipated in the main transformer below 1/6 of the total dissipated power, which means the maximum permitted power should be 3 W. This is our first important design input.

$$P_{trafo_MAX} = 3W \tag{16}$$

The maximum operating temperature is 55°C, as is typical for server applications. Due to the transformer safety isolation approvals, the maximum operating temperature of the transformer must be lower than 110°C, so:

$$\Delta T_{trafo_MAX} = (110 - 55)°C = 55°C \quad (17)$$

From (16) and (17) the max. thermal resistance of the core shape can be easily derived:

$$R_{th_trafo_MAX} = \frac{\Delta T_{trafo_MAX}}{P_{trafo_MAX}} = \frac{55}{3} °C/W = 18.3°C/W \quad (18)$$

Our selected core shape must have a thermal resistance lower than 18.3°C / W.

This requirement can be fulfilled through various methods; the preferred one will allow for maximizing the ratio between available winding area and effective volume, in line with equation (18).

Also, considering the power density target (in the range of 20 W / inch^3), the most suitable selection is

PQ 35/35, shown in Figure 15.

The related coil former shows a minimum winding area of 1.58 cm^2 and a thermal resistance of 16.5°C / W, as this is lower than the result from (18), it is thus able to dissipate up to 3.33 W by keeping the ΔT_{MAX} < 55°C.

Once verified that the thermal equations are fulfilled, we can proceed with the design of the primary and secondary windings and the core material selection with some important goals:

Fitting the geometry/overall dimensions of the core

Fulfilling the condition in (16)

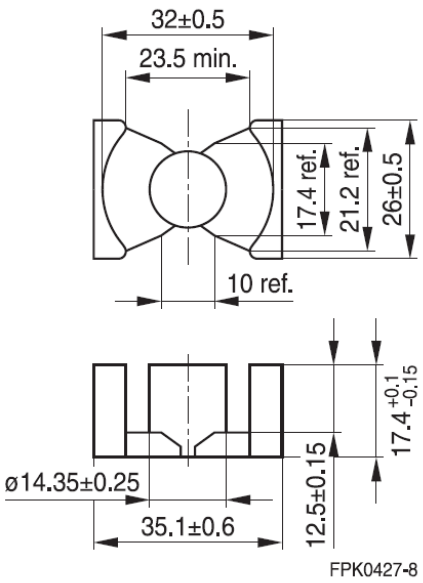
Try to split the losses between core and windings as equaly as possible: ideally a 50:50 ratio should be achieved at full load, but any ratio close to it would be acceptable.

- To IEC 62317-13
- Delivery mode: sets

Magnetic characteristics (per set)

$\Sigma l/A$ = 0.467 mm^{-1}
l_e = 79.20 mm
A_e = 169.7 mm^2
A_{min} = 146.5 mm^2
V_e = 13440 mm^3

Approx. weight 74 g/set



Dimensions in mm

Figure 15 TDK-Epcos PQ35/35 core

The selected core material is the ferrite TDK PC95, showing a very interesting plot of core losses (PCV) vs. flux density vs. frequency (see Figure 16).

The final structure of the main transformer is shown in Figure 17 below. This has been developed in cooperation with the partner company Kaschke Components GmbH, Göttingen - Germany

The primary is realized using a “sandwich” technique with 16 turns of 4 layers of Litz wire 45 strands 0.1 mm diameter This minimizes the AC losses due to skin and proximity effects. The secondary is made with a 20x0.5 mm copper band.

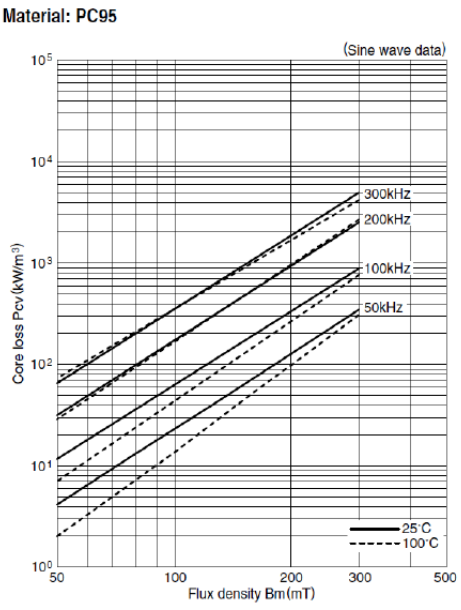


Figure 16 Ferrite core material TDK PC95

With this choice, at full load condition, the total copper losses (primary + secondary, DC+AC components) are 1.1 W and the core losses are 1.8 W, so overall:

$$P_{trafo} = P_{copper} + P_{core} = 2.9W < P_{trafo_MAX} = 3W \quad (19)$$

In other words, equation (19) fulfils the thermal equation (18)

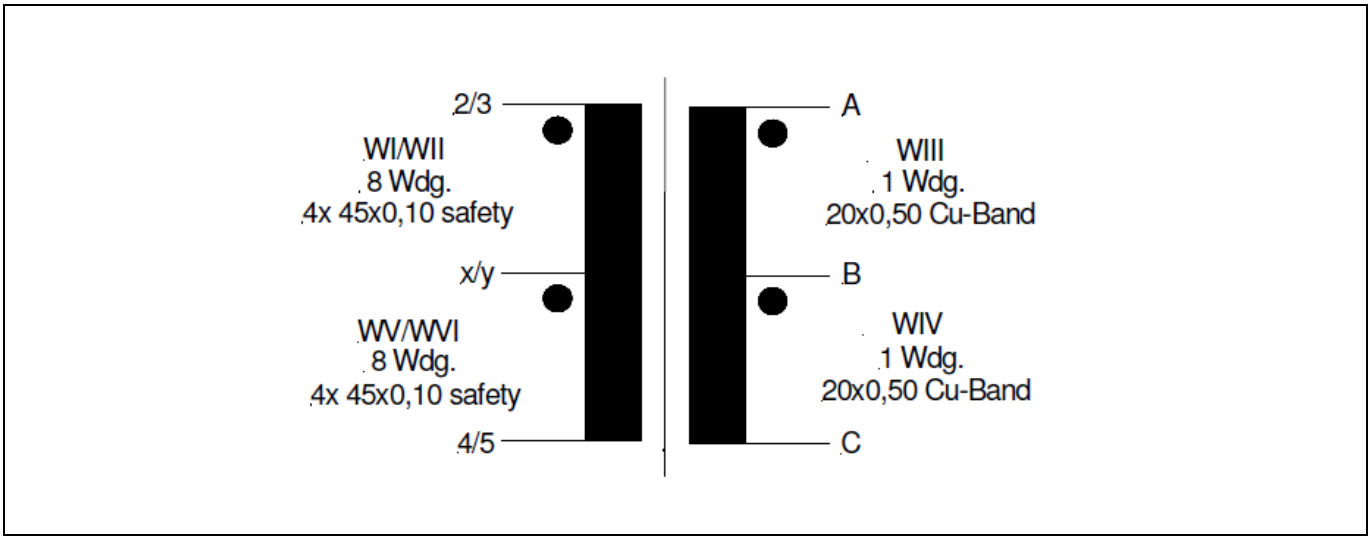


Figure 17 Winding structure of the PQ 35/35 LLC transformer (Kaschke Components GmbH)

An important transformer parameter involved in the LLC design is the primary or magnetizing inductance L_m, which, according to eq. (7), must be 195 µH. This value is obtained with distributed air gap on the side legs of the PQ core. This construction is preferred since it minimizes the effect of the "fringing flux" that generates additional losses in the windings close to the inner limb.

3.8 The resonant choke design

In LLC designs with stringent power density requirements, the resonant choke is normally embedded in the transformer as the leakage inductance is used for this purpose. This technique has the advantage of saving space and the cost of an additional magnetic component. It also has some drawbacks, including the challenge of controlling the value of L_r in mass production.

In this design, it has been decided to use an external L_r. This is because the demo board is intended to be primarily used for testing and benchmarking, and high power density is not the main focus. Having the resonant inductance externally allows a more flexible way of changing the resonant tank.

According to eq. (7), the overall value of L_r shall be 17 µH, including the contribution of the transformer primary leakage inductance.

The external resonant choke is realized using a RM-12 core and a winding construction that is illustrated in Figure 18 below and implemented by the partner company Kaschke Components GmbH Germany.

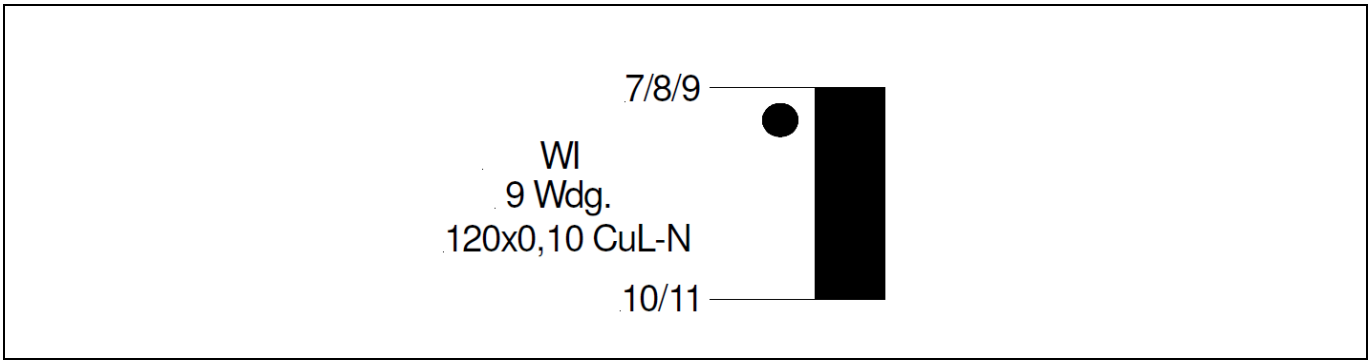


Figure 18 Winding structure of the RM12 resonant choke (Kaschke Components GmbH)

3.9 The synchronous rectification stage

In applications that target high efficiency both at low and high loads (such as 80PLUS Titanium), while often requiring high power densities, it is critical to select Synchronous Rectification (SR) stage MOSFETs that combine multiple key characteristics.

First of all, these SR MOSFETs should exhibit very low $R_{DS(on)}$. Indeed, due to the low voltages observed on the secondary side of server power supplies, large currents flow through the SR MOSFETs. Compared with other topologies such as ZVS phase-shifted full-bridge, using the LLC topology leads to increased peak currents for the SR MOSFETs, as well as higher RMS currents I_{RMS}.

The conduction losses P_{cond} of each SR MOSFET are given by:

$$P_{cond_SR} = R_{DS,on} \cdot (I_{RMS})^2 \quad (20)$$

These losses can only be mitigated through the use of a MOSFET with very low $R_{DS(on)}$.

Secondly, it is critical for these SR MOSFETs to exhibit low gate charges Q_g.

At light load, the switching losses of the SR MOSFETs dominate the conduction losses. For the LLC topology, the main contributor to these switching losses is Q_g.

Most of the time, a driving voltage of 12 V is applied to the SR MOSFETs. Although 12 V is not necessarily the optimized driving voltage, it is very popular in server PSUs because it is readily available. There is no need to derive it from another voltage rail. Therefore, we decided to follow this trend for the demo board by driving the SR MOSFETs with 12 V.

This requirement for low Q_g gives MOSFET manufacturers additional challenges, especially considering that SR MOSFETs also need to exhibit a very low $R_{DS(on)}$. This was possible for Infineon due to the new Infineon OptiMOS™ 40 V generation, where the gate charges have been significantly reduced in comparison with the previous generation.

Thirdly, the paralleled SR MOSFETs should turn on almost simultaneously.

This can be achieved by tightening the voltage threshold $V_{GS(th)}$ range. For the new OptiMOS™ 40 V generation, the datasheet guarantees a very narrow $V_{GS(th)}$ range, with min. and max. values equal to 1.2 V and 2.0 V respectively.

Finally, the MOSFET package is critical for a variety of reasons.

The package should exhibit low parasitic inductances in order to confine its contribution to the V_{DS} overshoot to a strict minimum. This is even more critical in server applications using the LLC topology, as the limited headroom for the V_{DS} overshoot between the transformer secondary voltage (25 V) and the 90% derating (36 V max) or even 80% derating (32 V max) applied to the V_{DS} of the SR MOSFETs;

Moreover, due to the conflicting requirements for high power density and high current capability, the package should combine a minimum footprint with good power dissipation.

Due to the high current densities arising at the source pins, which can lead to electromigration and thereafter destruction of the SR MOSFETs, the package should provide an enlarged source connection. While the first two points are addressed by standard SuperSO8 packages, it is the addition of source fused leads implemented in the new Infineon OptiMOS™ 40 V generation that reduce the high current densities mentioned above.

4 Board description

4.1 General overview

Figure 2 is the top view, bottom view and the assembly of 600 W HB LLC demo board. Key components are: **(1)** heatsink assembly of primary side switches IPP60R180P7 **(2)** Resonant capacitor **(3)** LLC analog controller ICE2HS01G **(4)** Resonant inductor **(5)** Main transformer **(6)** PCB assembly of the auxiliary circuit with bias QR Flyback controller ICE2QR2280Z **(7)** Heatsink assembly for cooling the synchronous rectifiers **(8)** Output capacitors **(9)** Output inductor **(10)** Half-bridge MOSFET gate driver 2EDL05N06PFG **(11)** Synchronous rectifier OptiMOS™ BSC010N04LS and **(12)** Dual channel gate driver 2EDN7524F used for synchronous rectifier MOSFETs.

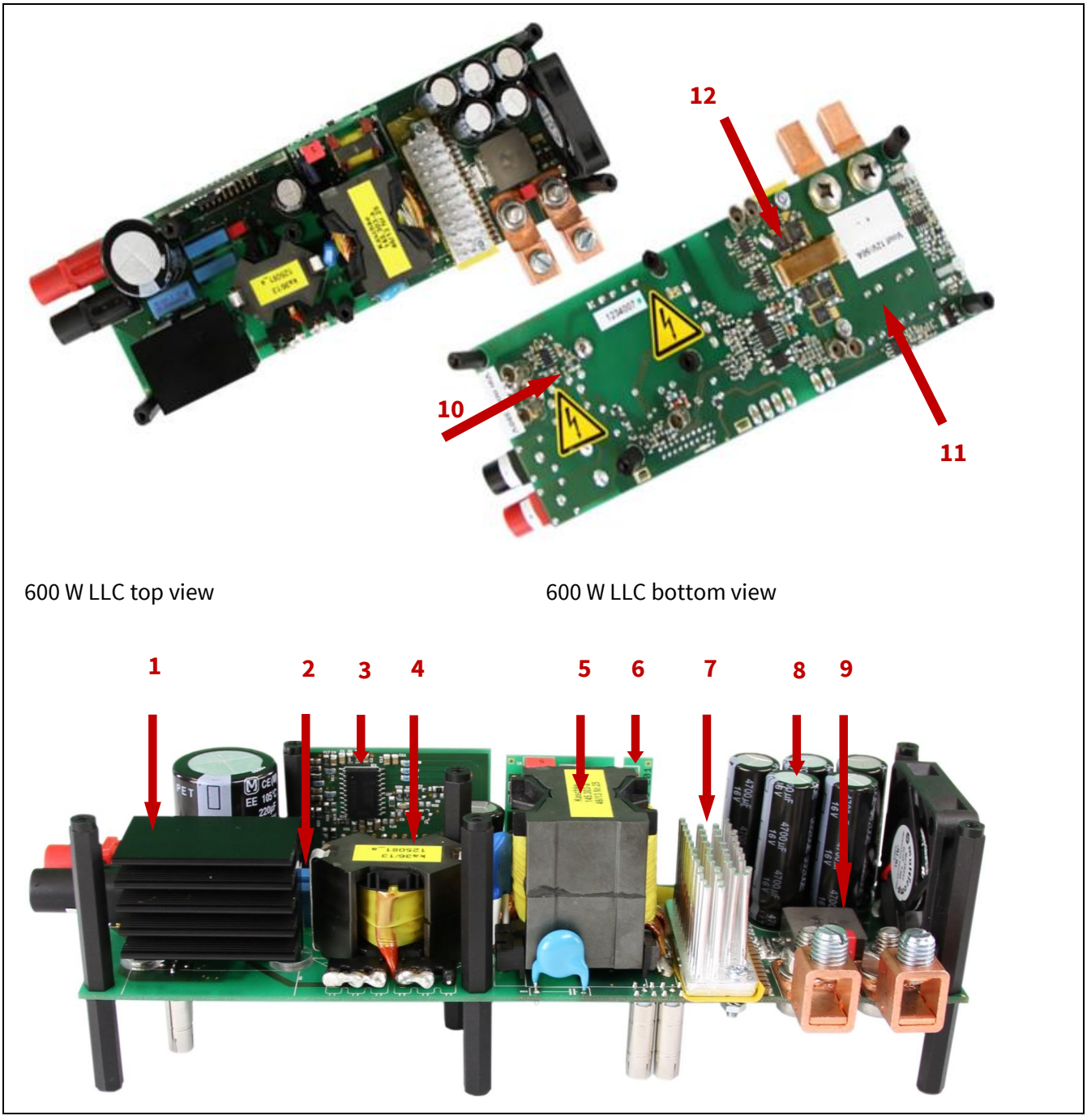


Figure 19 Infineon 600 W LLC demo board

4.2 Infineon components used in the board

This HB LLC 600 W demo board is a full Infineon solution meeting the highest efficiency standard 80PPLUS® Titanium using the following parts:

4.2.1 Primary HV MOSFETs CoolMOS™ IPP60R180P7

The CoolMOS™ 7th generation platform is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The 600 V CoolMOS™ P7 series is the successor to the CoolMOS™ P6 series. It combines the benefits of a fast switching SJ MOSFET with excellent ease of use, e.g. very low ringing tendency, outstanding robustness of body diode against hard commutation and excellent ESD capability. Furthermore, extremely low switching and conduction losses make switching applications even more efficient, more compact and much cooler.

Features:

- Suitable for hard and soft switching (PFC and LLC) due to an outstanding commutation ruggedness
- Significant reduction of switching and conduction losses
- Excellent ESD robustness >2 kV (HBM) for all products
- Better $R_{DS(on)}$/package products compared to competition enabled by a low $R_{DS(on)}$*A (below 1Ω*mm^2)
- Large portfolio with granular $R_{DS(on)}$ selection qualified for a variety of industrial and consumer grade applications according to JEDEC (J-STD20 and JESD22)

Benefits:

- Ease of use and fast design-in through low ringing tendency and usage across PFC and PWM stages
- Simplified thermal management due to low switching and conduction losses
- Increased power density solutions enabled by using products with smaller footprint and higher manufacturing quality due to >2 kV ESD protection
- Suitable for a wide variety of applications and power ranges

Applications:

- PFC, hard switching PWM and resonant switching power stages. e.g. PC Silverbox, adapter, LCD & PDP TV, lighting, server, telecom and UPS.

4.2.2 LLC analog controller ICE2HS01G

ICE2HS01G is Infineon's second generation half-bridge LLC controller designed specifically for high efficiency half-bridge or full-bridge LLC resonant converters with SR control for the secondary side. With its new driving techniques, SR can be realized for LLC converters operated with secondary switching current in both CCM and DCM conditions. No special SR controller IC is required on the secondary side. Maximum switching frequency is supported up to 1 MHz. Apart from the patented SR driving techniques, this IC provides a very flexible design and integrates full protection functions as well. It is adjustable for maximum/minimum switching frequency, soft-start time and frequency, dead time between primary switches, turn-on and turn-off delay for the secondary SR MOSFETs. The integrated protections include input voltage brownout, primary three-level over current, secondary overload protection and no load regulation. It also includes a burst mode function which

offers an operation with low quiescent current maintaining high efficiency at low output load while keeping output ripple voltage low.

4.2.3 HB gate driver 2EDL05N06PFG

Developers of consumer electronics and home appliances strive continuously to achieve higher efficiency in applications and smaller form factors. One area of interest in power supply design is the switching behaviour and power losses of new power MOSFETs, such as the latest generations of CoolMOS™ with dramatically reduced gate charges, as they can be optimized by dedicated driver ICs.

The 2EDL05N06PFG IC is one of the drivers from Infineon's 2EDL EiceDRIVER™ compact 600 V half-bridge gate driver IC family with a monolithic, integrated, low-ohmic and ultrafast bootstrap diode. Its level shift SOI technology supports higher efficiency and smaller form factors within applications. Based on the SOI-technology, there is excellent ruggedness for transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch-up will occur at any temperature or voltage condition. The outputs of the two independent drivers are controlled at the low-side using two different CMOS resp. LS TTL compatible signals, down to 3.3 V logic. The device includes an under voltage detection unit with a hysteresis characteristic, which is optimized for either IGBTs or MOSFETs. 2EDL05N06PF (DSO-8) and 2EDL05N06PJ (DSO-14) are driver ICs with under voltage lockout for MOSFETs. These two parts are recommended for server/telecom SMPS, low voltage drives, e-Bike, battery charger and half-bridge based switch mode power supply topologies.

4.2.4 Advanced dual channel gate driver 2EDN7524F

The fast dual channel 5 A non-isolated gate driver is an advanced dual-channel driver optimized for driving both standard and SJ MOSFETs, as well as Gallium Nitride (GaN) power devices, in all applications in which they are commonly used. The input signals are TTL compatible with a high voltage capability up to 20 V and down to -5 V. The unique ability to handle -5 V_{DC} at the input pins protects the IC inputs against ground bounce transients.

Each of the two outputs is able to sink and source current up to 5 A, utilizing a true rail-to-rail stage, that ensures very low impedances of 0.7 Ω up to the positive rail and 0.55 Ω down to the negative rail. Very low channel to channel delay matching (typically 1 nS) is implemented, which enables the double source and sink capability of 10 A by paralleling both channels.

Different logic input/output configurations guarantee high flexibility for all applications; e.g. with two paralleled switches in a boost configuration. The gate driver is available in 3 package options: PG-DSO-8, PG-VDSON-8 and PG-TSDSO-8-X (size minimized DSO-8).

Main features

- Industry standard pinout
- Two independent low-side gate drivers
- 5 A peak sink/source output driver at V_{DD} = 12 V
- True low impedance rail-to-rail output (0.7 Ω and 0.5 Ω)
- Enhanced operating robustness due to high reverse current capability
- -10 V_{DC} negative input capability against GND bouncing
- Very low propagation delay (19 nS)
- Typ. 1 ns channel to channel delay matching

- Wide input and output voltage range up to 20 V
- Active low output driver even on low power or disabled driver
- High flexibility through different logic input configurations
- PG-DSO-8, PG-VDSON-8 and TSSOP-8 package
- Extended operation from -40°C to 150°C (junction temperature)
- Particularly well suited for driving standard MOSFETs, SJ MOSFETs, IGBTs or GaN power transistors

4.2.5 Bias QR Flyback controller ICE2QR2280Z

ICE2QRxxxx is a second generation quasi-resonant PWM CoolSET™ with a power MOSFET and startup cell in a single package optimized for offline power supply applications such as LCD TV, notebook adapters and auxiliary/housekeeping converters in SMPS. The digital frequency reduction with decreasing load enables a quasi-resonant operation down to very low load. As a result, the average system efficiency is significantly improved compared to conventional solutions. The active burst mode operation enables ultra-low power consumption in standby mode operation and low output voltage ripple. The numerous protection functions give a full protection of the power supply system in failure modes. The main features of the ICE2QR2280Z that make it suitable as an auxiliary converter for this LLC demonstration board are:

- High voltage (650 V/800 V) avalanche rugged CoolMOS™ with startup cell
- Quasi-resonant operation
- Load dependent digital frequency reduction
- Active burst mode for light load operation
- Built in high voltage startup cell
- Built in digital soft-start
- Cycle-by-cycle peak current limitation with built in leading edge blanking time
- Foldback point correction with digital sensing and control circuits
- V_{CC} undervoltage and overvoltage protection with autorestart mode
- Overload / open loop protection with autorestart mode
- Built in over temperature protection with autorestart mode
- Adjustable output overvoltage protection with latch mode
- Short winding protection with latch mode
- Maximum on time limitation
- Maximum switching period limitation

4.2.6 SR MOSFETs OptiMOS™ BSC010N04LS

For the SR stage, the selected device is BSC010N04LS, from the latest OptiMOS™ 40 V family. SR is naturally the best choice for high efficiency LLC designs with low output voltage and high output current, as in this demo board. In applications that target high efficiency at both light and heavy loads – such as 80PLUS® Titanium while often requiring high power densities, it is critical to select SR MOSFETs that combine following key characteristics:

- Very low $R_{DS(on)}$: BSC010N04LS provides the industry's first 1 mΩ 40 V product in a SuperSO8 package
- Low gate charge Q_g, which is important in order to minimize driving losses, with benefits for light load efficiency

- Very tight $V_{GS(th)}$ range: when paralleling this allows the MOSFETs to turn-on almost simultaneously. Selected OptiMOS™ offer very close min. and max. values of $V_{GS(th)}$, respectively 1.2 V and 2 V
- Monolithically integrated Schottky like diode, to minimize associated conduction losses
- Package; the BSC010N04LS in SuperSO8 with source fused leads is able to address all of the typical crucial requirements for a suitable SR MOSFET package:
  - Minimizing parasitic inductances
  - Combining compact footprint with good power dissipation
  - Enlarged source connection in order to minimize the occurrence of electromigration.

4.3 Board schematics

4.3.1 Mainboard schematic

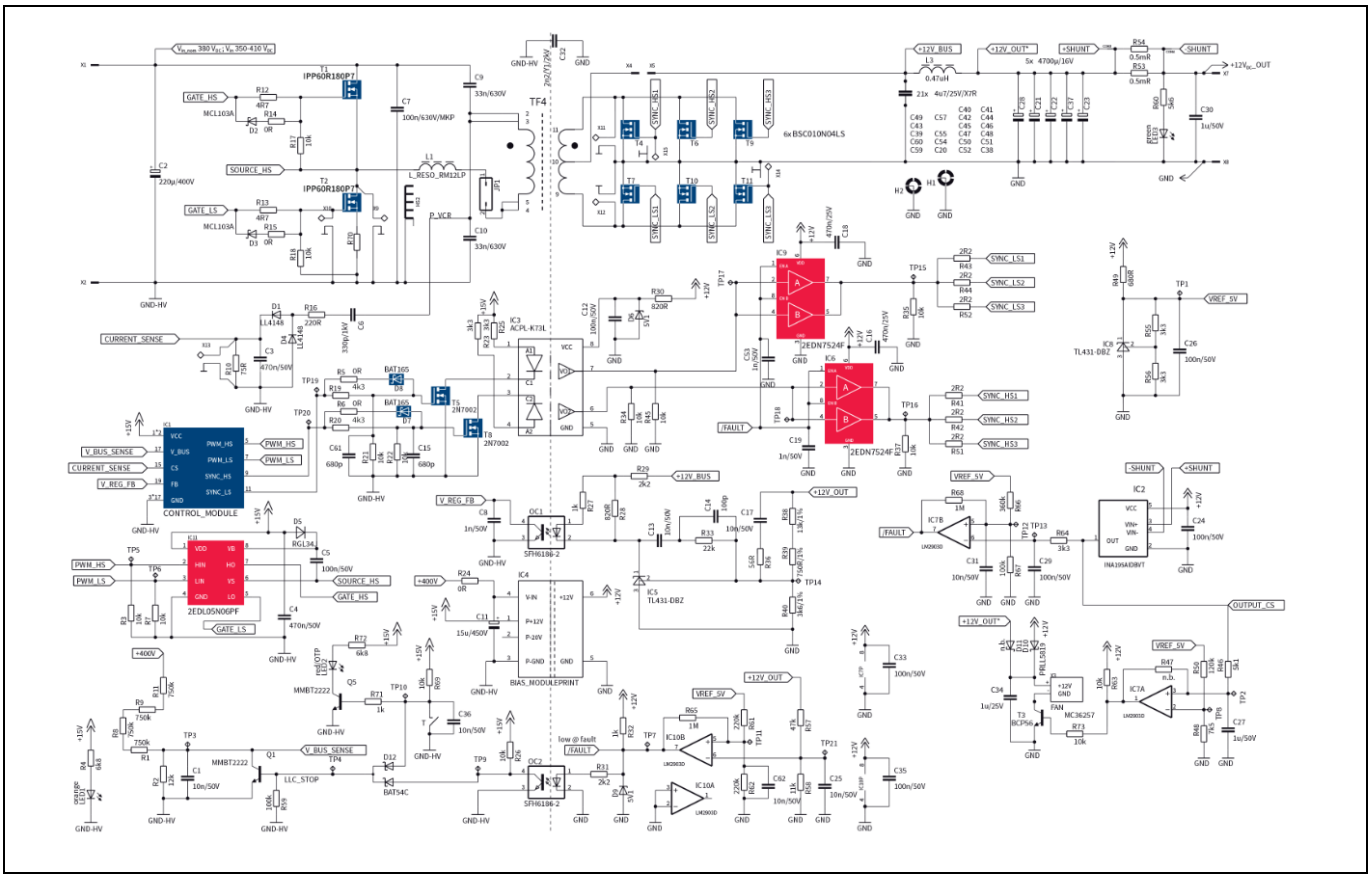


Figure 20 Mainboard schematic

4.3.2 Controller board schematic

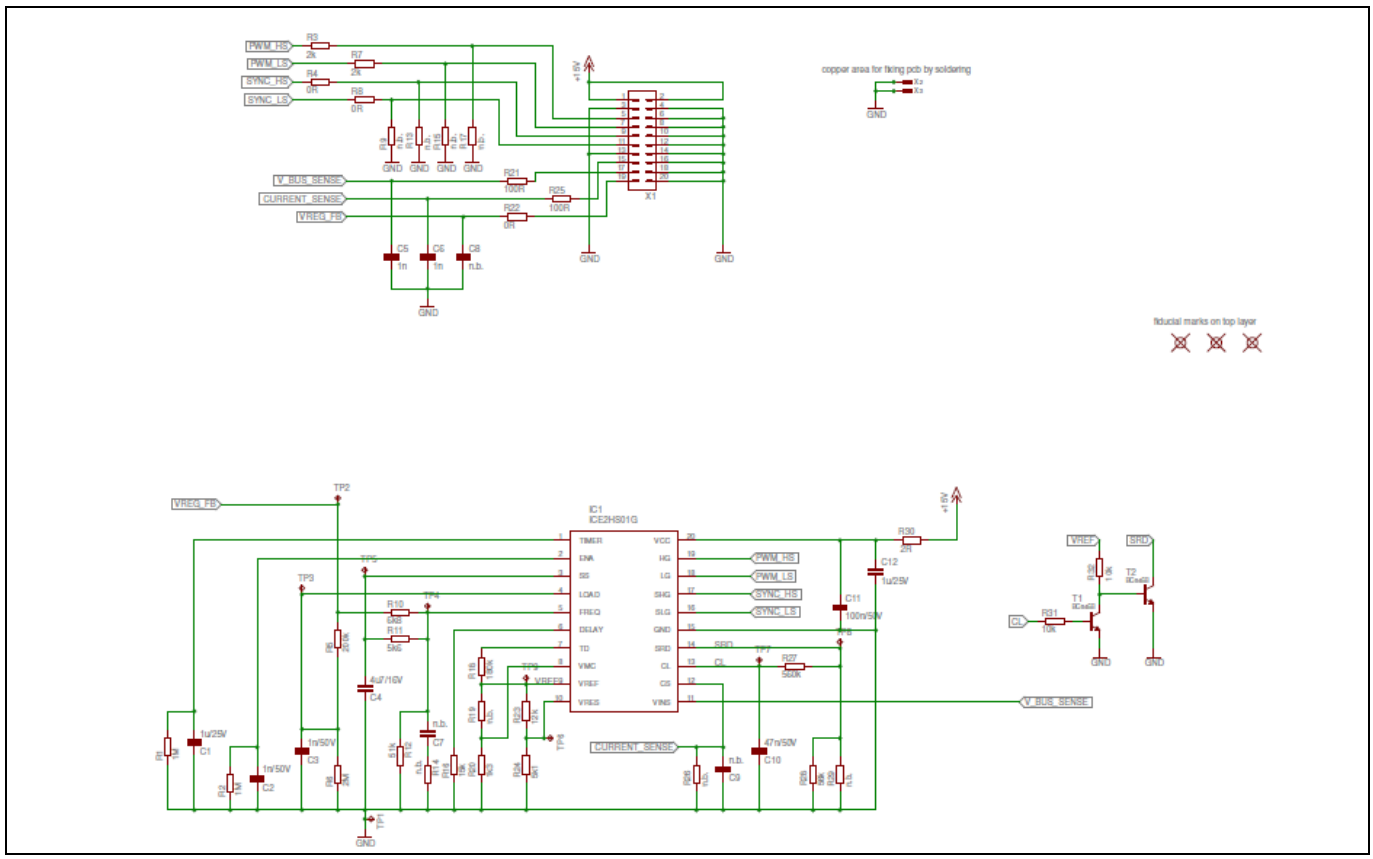


Figure 21 Controllerboard schematic

4.3.3 Bias board schematic

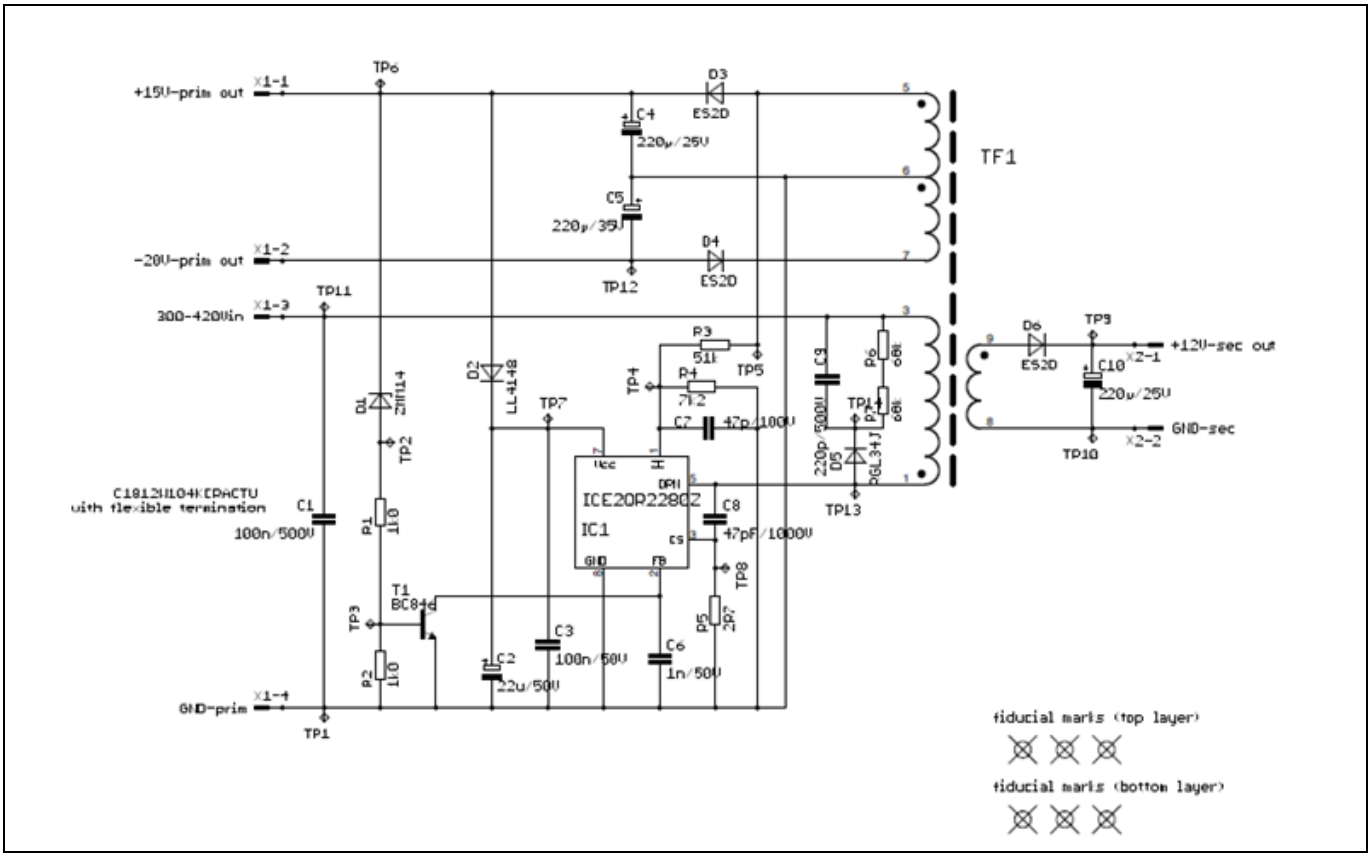


Figure 22 Bias board schematic

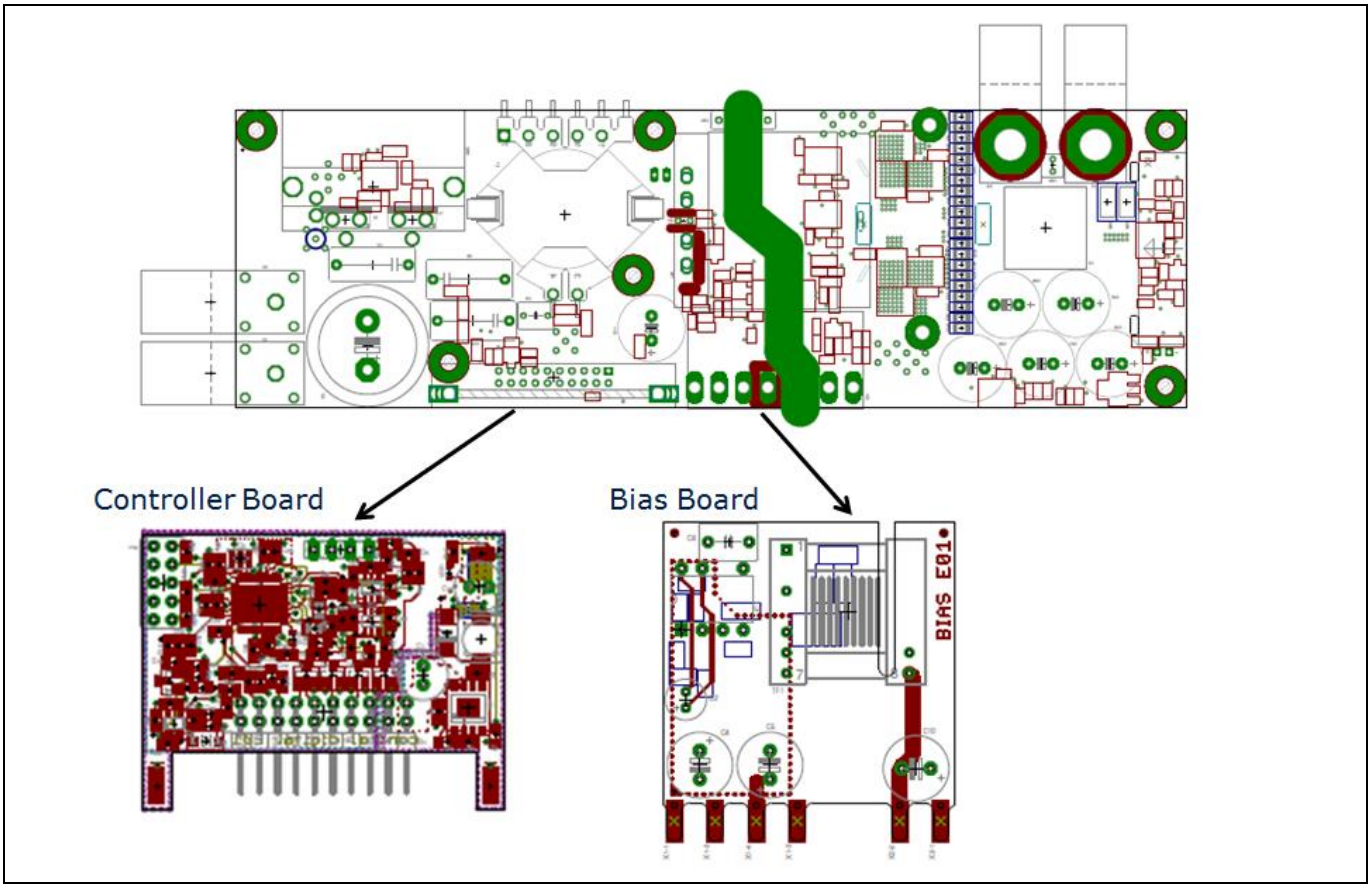


Figure 23 Mainboard PCB with controller – and bias board

4.4 Critical LLC operation - hard commutation

In LLC converters, hard commutation of the body diode can occur during start-up, burst mode, overload and short circuit conditions. This condition can be prevented during design by using a proper control technique, a correct selection of resonant components and a proper setting of the minimum and maximum operating frequency. Hard commutation occurs in LLC converters during the commutation period of the body diode. During this time, resonant inductor current is flowing through body diode of the MOSFET creating a ZVS condition upon this MOSFET's turn-on. When the current is not able to change its direction prior to the turn-on of the other MOSFET, more charge will be stored in the P-N junction of that MOSFET. When the other MOSFET turns on, a large shoot through current will flow due to the reverse recovery current of the body diode. This results in a high reverse recovery peak current I_{RRM} and high reverse recovery dV/dT, which could sometimes lead to MOSFET breakdown. This operation is widely explained in technical literature [5, 7].

In the 600 W LLC analog controlled demo board, only the burst mode condition (described in detail in the following paragraph) tends to lead to hard commutation.

The event shown in Figure 24 was captured only once during a start-up in burst mode operation and this is not easy to reproduce.

In fact, the drain current in the low-side MOSFET is not able to change direction, thus inducing hard commutation during the turn-off of the high side switch. However, the V_{DS_peak} is 474 V, so within the 80% derating even during this abnormal condition, despite the huge current spike. In addition, V_{GS_MAX} is only 23.2 V -

well below the allowed data sheet limit. We can conclude that the IPP60R180P7 is able to withstand this condition without any problem.



Figure 24 Hard commutation during burst mode operation, V_{DS_pk} , $V_{GS_max/min}$ and I_{DS_MAX}

For the sake of completeness, it should be stated that in a broad range of applications the voltage spike on the gate and drain may vary depending on the layout quality and parasitics. In some cases, a different selection of turn-on and turn-off gate resistors may be needed in order to keep V_{GS} and V_{DS} within an acceptable range. Even a possible R_g change in the range of ±10 Ω will not significantly affect the efficiency, due to the CoolMOS™ P7 technology switching behavior.

It is important to highlight that the condition described in Fig.24 is the real worst case we have been able to capture in the 600 W HB LLC demo board using analog control. There are no other observed hard commutation events during start-up, nor during output short circuit conditions.

4.5 ZVS behaviour analysis

Nearly full ZVS is achieved on the entire output load range as shown in Figure 25.

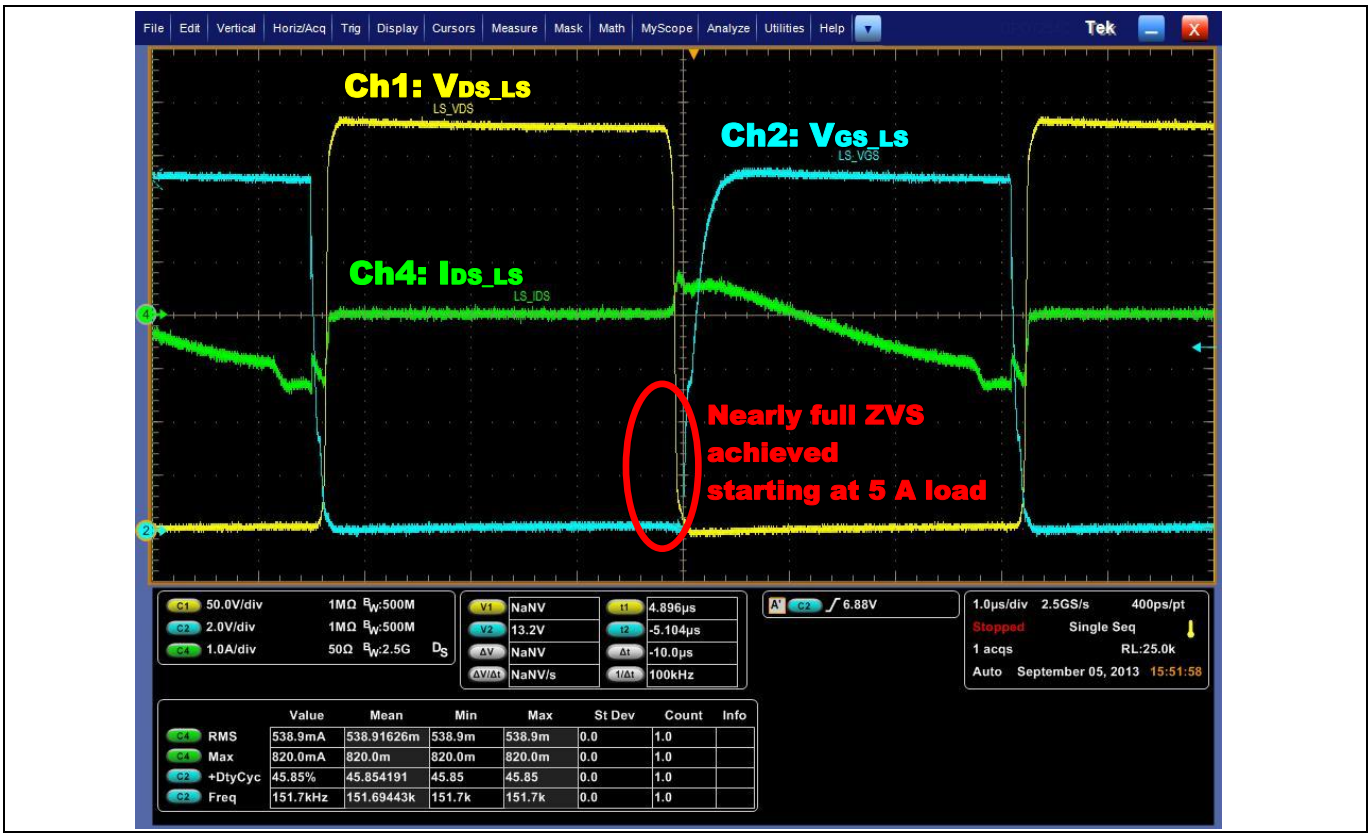


Figure 25 Nearly full ZVS starting at 5 A load

4.6 Burst mode operation

At no load or a very light load condition, the LLC controller provides a frequency approaching its maximum setting. In this condition, in order to achieve full ZVS, the magnetizing current should be high enough to discharge the output capacitances. Due to the magnetizing current limitation, switching loss (especially turn-off loss) is relatively high if the devices continue to switch at the highest frequency. In order to overcome this phenomenon, the burst mode function is enabled and implemented. This results in lower switching losses and driving losses, due to the low burst frequency.

Additionally, this helps to achieve regulation even in a no load condition, preventing challenges often seen in LLC converters in that condition. These regulation problems are typically due to parasitic components such as the primary to secondary main transformer coupling capacitance and the SR MOSFET's output capacitance. The combination of these factors generates the third resonant frequency in the LLC gain curve, making the converter virtually uncontrollable at no load. The burst mode overcomes this problem, by limiting the unwanted primary to secondary power transfer, due to these parasitic effects.

For further details about this operation of the LLC converter, please refer to the specific literature [8].

The waveforms in Figure 26 illustrate the burst mode technique applied in our 600 W LLC demo board.

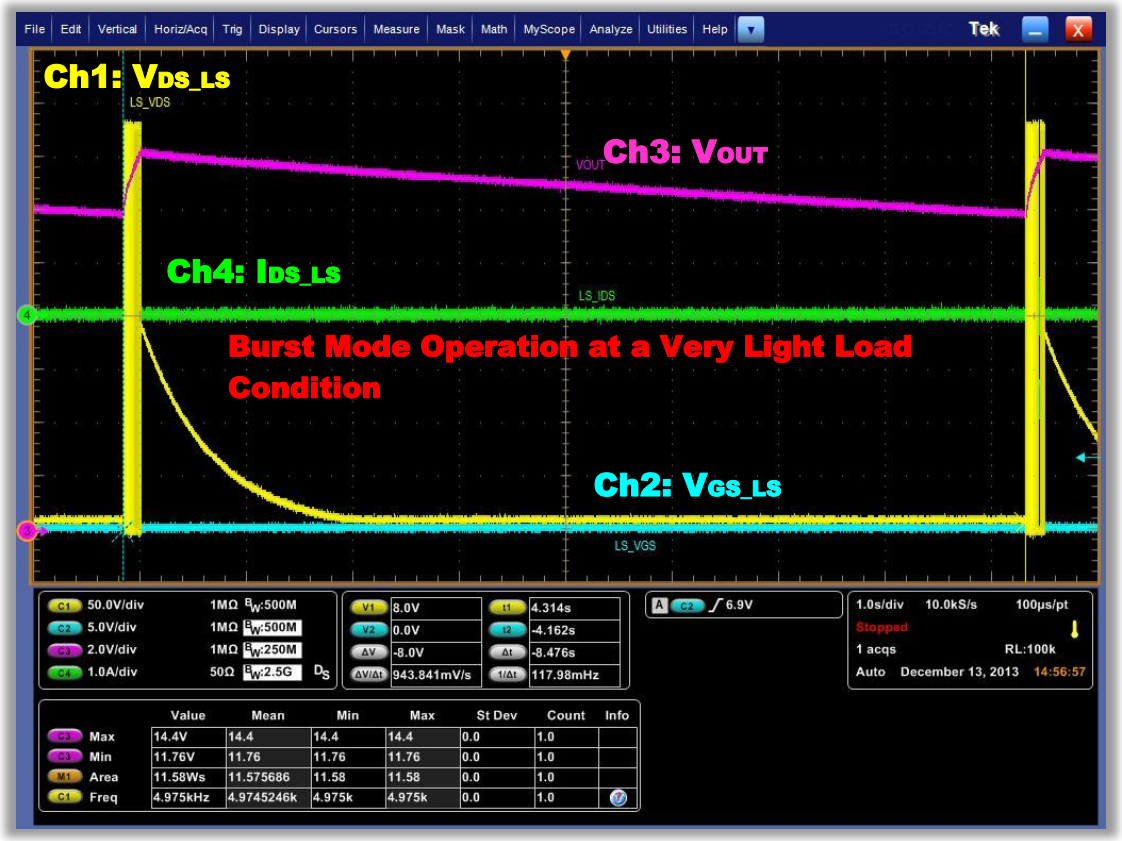


Figure 26 Burst mode operation at no-load and very light load condition

4.7 Efficiency

4.7.1 80+ Titanium efficiency target

Figure 27 shows the efficiency measurement performed on the 600 W LLC demo board using an IPP60R180P7 with reference to the 80+ Titanium standard efficiency (dotted blue line). The Titanium standard fixes the minimum efficiency requirement at the three most important load conditions in a computing / server application, 10%, 50% and 100%.

The combination of proper converter design (including the resonant tank and transformer) and HV device selection allows meeting (with a reasonable margin) the efficiency targets especially in the 10-40% load range.

Proper selection of LV SR devices and secondary side design influences the performance more in the 40-100% load range.

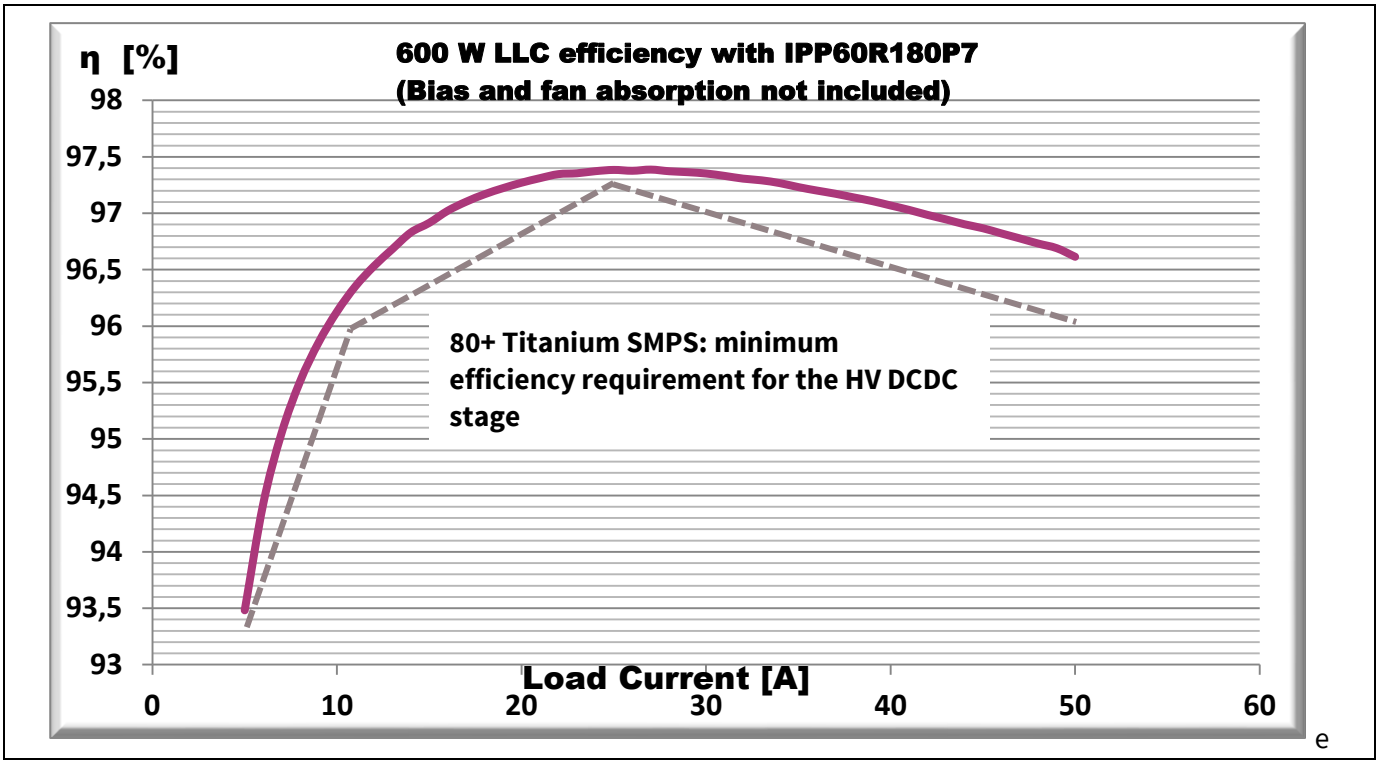


Figure 27 Infineon P7 based 600 W LLC demo board efficiency vs Titanium standard efficiency

The measurement is performed in a fully automated setup, as shown in Fig. 28, according to the guidelines included in [9]. The total accuracy of the measurement chain is in the ±0.1% range.

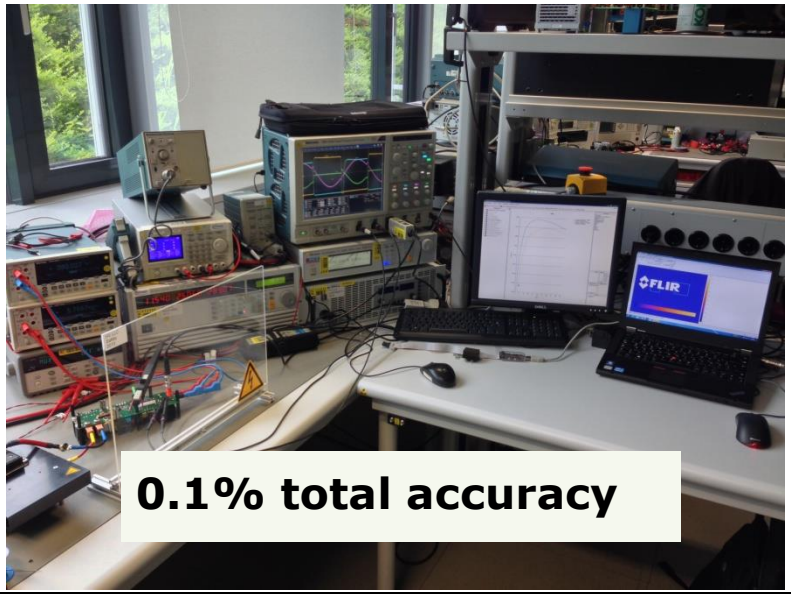


Figure 28 Infineon 600 W LLC automated efficiency measurement setup

4.7.2 Losses breakdown

Along with the efficiency plot shown in the previous paragraph, it is interesting to analyse the losses breakdown between the different components of the demo board. Figures 29, 30 and 31 below provide this overview.

The contribution of the primary MOSFETs progressively increases from light to heavy load. On the other hand, the contribution of the main transformer is important at 10% load, but it tends to decrease at higher load. This is mainly due to the core losses (higher at light load due to higher switching frequency) and the magnetizing inductance, which is almost constant and independent to the load. In fact, this feature allows the HB LLC topology to easily achieve ZVS down to very light load and definitely differentiates the HB LLC topology from other soft switching approaches, such as the ZVS phase-shift full-bridge.

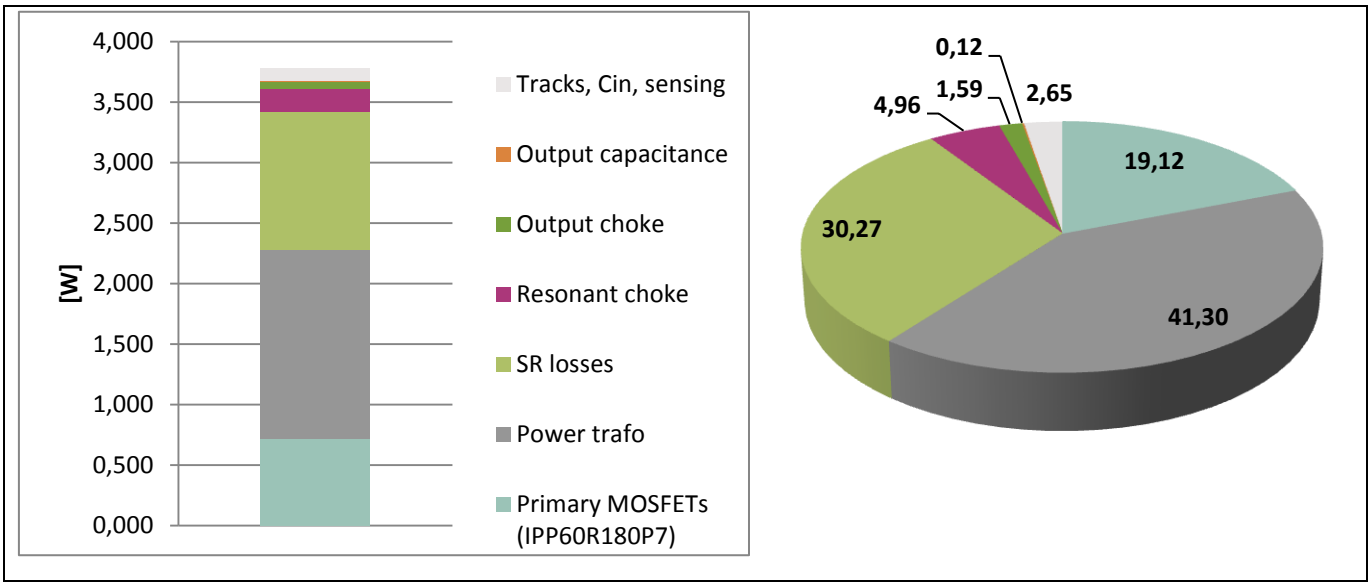


Figure 29 10% P_{max} overall load losses breakdown

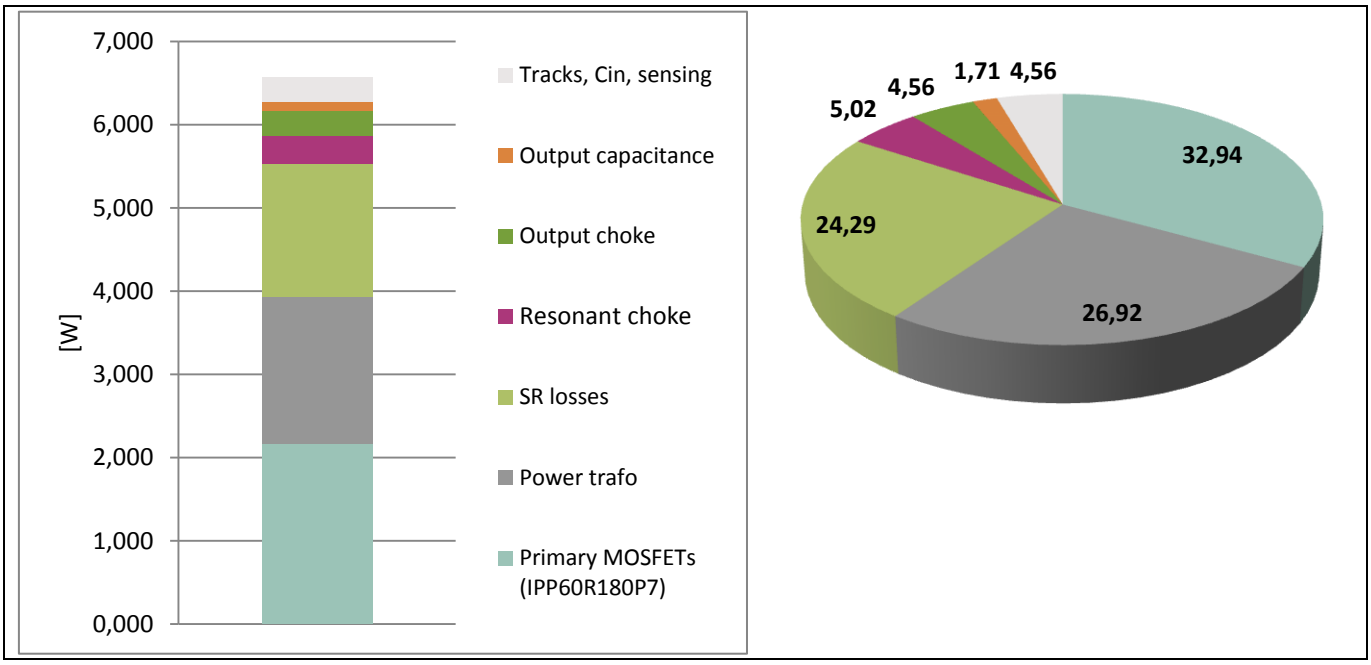


Figure 30 50% P_{max} overall load losses breakdown

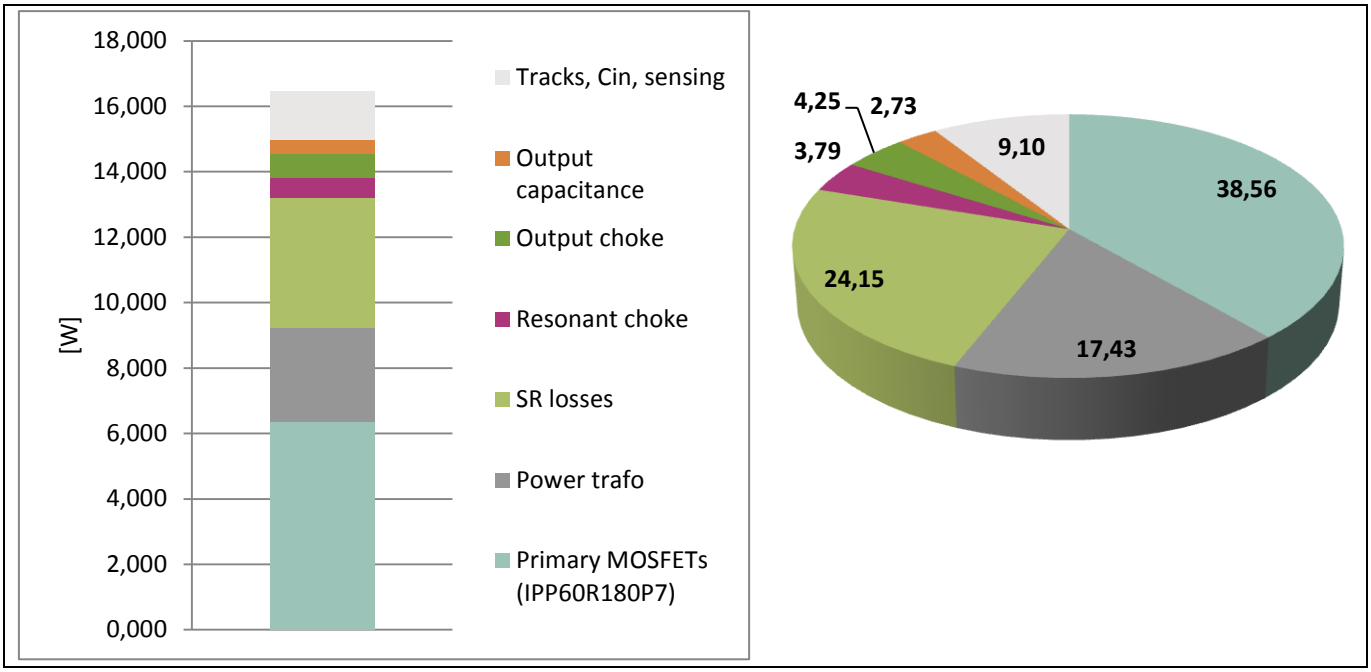


Figure 31 100% P_{max} overall load losses breakdown

5 Conclusion

This document has described the 600 W HB LLC demo board, its principle of operation and its concept along with the most important choices made in its design.

It has been demonstrated that the proper selection of primary HV MOSFETs and secondary MV MOSFET in the SR stage, along with a suitable design of the transformer and resonant tank and a control technique that achieves a level of efficiency for the HV DC/DC stage to be able to fulfil the 80+ Titanium standard at the complete PSU level.

The features of the new 600 V CoolMOS™ P7 have been deployed through a valuable application example provided by our board.

Specifically, the excellent switching FOM, due to the reduced gate charge and turn-off losses, is the key enabler for the very high efficiency down to 10% load, as per 80+ Titanium requirements.

The low typical $R_{ds(on)}$ is the main reason why P7 shows high efficiency in the range 50-100% load, where the conduction losses are the predominant HV MOSFET loss mechanism in the HB LLC topology.

Moreover, the ruggedness of P7 technology has been demostrated in some of the HB LLC critical operating conditions, where the primary HV MOSFETs are submitted to heavy stress, especially in designs where the converter control (e.g. analog) is not able to prevent these unpredictable events.

6 Test/power-up procedure

Test	Test procedure	Condition
1. Auxiliary circuit turn-on	Apply 30 V_{DC} on the input.	V_{in}: ~30 V_{DC}
		Orange LED will light up
2. LLC converter turn-on	Apply 350 V_{DC} converter will give V_{out} =12 V_{DC}	V_{in}: 350 V_{DC}
		V_{out}:12 V
3. Operational switching frequency	Using a voltage probe, monitor switching frequency at following test conditions:	V_{in}:380 V_{DC}
		V_{out}:12 V
	@5 A output load 10% load - ~ 155 kHz*	I_{out}: 5 A
	@25 A output load 50% load - ~ 142 kHz*	I_{out}: 25 A
	@50 A output load 100% load - ~ 132 kHz*	I_{out}: 50 A
	(*measure freq. at “Pri_LS_VGS“- connector; +-10 kHz)	
4. Fan enable	Switch the load from 50 A to 5 A. Increase the output load current from 11-14 A, fan should turn on.	V_{in} = 380 V_{DC}
		I_{out} = 5 A
		ÞFan is off
		V_{in} =380 V_{DC}
		I_{out} = 11-14 A
		ÞFan is on
5. Switch off input start-up at no load	Switch off the input	V_{in} = 0 V_{DC}
		I_{out} = 0 A
	Switch at 380 V_{DC} on **no load output**. Operation should be in burst mode.	V_{in} = 380 V_{DC}
		I_{out} = 0 A
		V_{out} = 11.5 – 12.5
6. Switch off input start-up at full load	Switch off the input	V_{in} = 0 V_{DC}
		I_{out} = 0 A
	Apply 380V_{dc} with full load @50 A output. V_{out} is in between 11.8 – 12.2 V_{DC}* *(*measure on the board-connector)*	V_{in} = 380 V_{DC}
		V_{out}: 11.8 – 12.3 V_{DC}
		I_{out} = 50 A
7. Running no load -> output short circuit	Switch off load from 380 V_{DC} **50 A** to 380 V_{DC} **0 A**.	Vin = 380 V_{DC}
	Short circuit the load using the short circuit function of the e-load. **Converter should latch.**	(after short circuit) **V_{out} = 0 V_{DC}**
		I_{out} = 0 A
8. Switch off input & remove short circuit	Switch off the Input.	V_{in} = 0 V_{DC}
9. Running full load -> over current protection	Remove short circuit function on the load.	I_{out} = 0 A
	Apply 380 V_{DC} 50 A with full load output. Increase the current on the output 1 A each step until the converter goes into protection	V_{in} = 380 V_{DC}
		I_{out} = 50 A

	starting from 50 A. OCP occurs between 55 A and 62 A.	OCP = between 55 A – 62 A
10. Running full load -> output short circuit	Apply 380 V_{DC} 50 A with full load output. Short circuit the load using the short circuit functions of the load. Converter should latch.	I_{out} = 0 A
		V_{in} = 380 V_{DC}
		I_{out} = 50 A
		(after short circuit) **V_{out}=0 V_{DC}**
11. Switch off input; start-up -> output short circuit	Switch off the input.	V_{in}= 0 V_{DC}
		I_{out} = 0 A
	Apply 380 V_{DC} with output load short circuit. *Converter should be in hiccup/latch mode.*	V_{in} = 380 V_{DC}
		I_{out} = short circuit
		V_{out} = 0 V short circuit (hiccup/latch)
12. Switch off input & remove short circuit	Switch off the Input.	V_{in}= 0 V_{DC}
	Remove short circuit function on the load.	I_{out} = 0 A
13. Dynamic loading	Apply 380 V_{DC}. Set the electronic load to dynamic loading mode with the following settings:	V_{in} = 380 V_{DC}
	CCDH1: I_{out} 5 A	I_{out} = 5 A…50 A
	CCDH2: I_{out} 50 A	V_{out} = 11.5 – 12.5 V_{DC}
	Dwell time: 10 ms	
	Load slew rate: 1 A/µS	

7 Useful material and links

The following links provide more detailed information about the devices from Infineon used and the magnetic components.

- Primary HV MOSFETs CoolMOS™ IPP60R180P7
  www.infineon.com/600v-p7
- LLC analog controller ICE2HS01G
  http://www.infineon.com/dgdl/ICE2HS01G_PDS_v2.1_20110524_Public.pdf?folderId=db3a304412b407950112b408e8c90004&fileId=db3a30432a40a650012a458289712b4c
- HB gate drive 2EDL05N06PFG
  http://www.infineon.com/dgdl/Infineon-2EDL05x06xx-DS-v02_05-EN.pdf?fileId=db3a30433e30e4bf013e3c649ffd6c8b
- Advanced dual channel gate drive 2EDN7524F
  http://www.infineon.com/dgdl/Infineon-2EDN752x_2EDN852x-DS-v01_00-EN.pdf?fileId=5546d4624cb7f111014d672f9fbb5142
- Bias QR Flyback controller ICE2QR2280Z
  http://www.infineon.com/dgdl/Datasheet_ICE2QR2280Z_v21_20110830.pdf?folderId=db3a304412b407950112b408e8c90004&fileId=db3a30432a7fedfc012a8d8038e00473
- SR MOSFETs OptiMOS™ BSC010N04LS
  http://www.infineon.com/dgdl/BSC010N04LS_rev2.0.pdf?folderId=db3a304313b8b5a60113cee8763b02d7&fileId=db3a3043353fdc16013552c1c63647c4
- Main transformer and resonant choke ferrite cores
  http://en.tdk.eu/blob/519704/download/2/ferrites-and-accessories-data-book-130501.pdf

8 References

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[2] F. Di Domenico, J. Hancock, A. Steiner, J. Catly, P. Yelamos, A. Medina “600 W Halfbridge LLC eval board with 600 V CoolMOS™ C7 and digital control by XMC™”, Infineon Technologies, May 2016

[3] Sam Abdel Rahman: “Resonant LLC Converter: Operation and Design: 250W 33Vin 400V_{out} Design Example”, Infineon Technology AN 2012

[4] Alois Steiner, Francesco Di Domenico and others: “600 W Half Bridge LLC Evaluation Board with 600 V CoolMOS™ C7”, Infineon Technologies AN 2015

[5] Lawrence Lin, Gary Chang: “Consideration of Primary side MOSFET Selection for LLC topology”, Infineon Technologies AN 2014

[6] Liu Jianwei, Li Dong: “Design Guide for LLC Converter with ICE2HS01G”, Infineon Technologies AN V1.0, July 2011

[7] Francesco Di Domenico, David Meneses Herrera, Stefano de Filippis: “3kW dual-phase LLC demo-board using 600 V CoolMOS™ P7 and digital control by XMC4400.” Infineon Technologies AN, 2017

[8] Jae-Hyun Kim, Chong-Eun Kim and others: “Analysis for LLC Resonant Converter Considering Parasitic Components at Very Light Load Condition”, 8th International Conference on Power Electronics, 2011 – Korea

[9] Dr. Arshad Mansoor, Brian Fortenbery, Peter May-Ostendop and others: “Generalized Test Protocol for Calculating the Energy Efficiency of Internal Ac-Dc and Dc-Dc Power Supplies”, Revision 6.7, March 2014

9 List of abbreviations

BOM	Bill Of Materials
C_{GD}	Internal Gate Drain capacitance $C_{GD}=C_{rss}$
C_{iss}	input capacitance $C_{iss}=C_{GS}+C_{GD}$
$C_{o(er)}$	effective output capacitance
C_r	resonant capacitance
di/dt	steepness of current slope at turn off / turn on
DUT	device under test
dv/dt	steepness of voltage slope at turn off / turn on
E_{off}	energy losses at switch off
E_{on}	energy losses loss at switch on
E_{oss}	stored energy in output capacitance (C_{oss}) at typ. V_{DS}=400V
FHA	First Harmonic Approximation Method
FOM	Figures of Merit
f_r	resonant frequency
I_D	drain current
I_{RMS}	effective root mean square current
I_{mag}	magnatizing current
$I_{m,pk}$	peak magnetizing current
K	gain factor
L_r	resonant inductance
L_m	magnetizing inductance
m	inductance factor
N_p	primary winding
N_S	secondary winding
n	transformer turn ratio
MOSFET	metal oxide semiconductor field effect transistor
P_{cond_SR}	synchronous rectification conduction losses
PFC	power factor correction
PNP	bipolar transistor type (pnp vs. npn)
Q_{OSS}	Charge stored in the C_{OSS}
Q	quality factor
R_{ac}	total equivalent resistor
$R_{DS(on)}$	drain-source on-state resistance
$R_{g,tot}$	total gate resistor
R_o	output resistor
R_{th}	thermal resistance
t_{dead}	dead time
t_{ecs}	early channel shut down time
V_{DS}	drain to source voltage, drain to source voltage
$V_{gs,th}$	drain to source threshold voltage
V_{O_AC}	output voltage, alternating current
V_{In_AC}	input voltage, alternating current
V_{In_nom}	nominal input voltage
V_{out_nom}	nominal output voltage
ZCS	zero current switching
ZVS	zero voltage switching

Table 2

Revision History

Major changes since the last revision

Page or Reference	Description of change
--	First Release

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